NIKOS HARDAVELLAS

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Computer Science & Electrical and Computer Engineering
McCormick School of Engineering, Northwestern University
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RESEARCH INTERESTS

Parallel systems, computer architecture, microarchitecture, nanophotonics-based computer architectures, memory systems, design for dark silicon, memory-oriented system design, quantum computer systems.

APPOINTMENTS

Northwestern University, 2009–present
Professor
Department of Computer Science, and
Department of Electrical and Computer Engineering – Computer Engineering Division
McCormick School of Engineering and Applied Science

Ministry of Development and Investments, 2021–present
Independent Expert
Hellenic Foundation for Research & Innovation (HFRI)
General Secretariat for Research and Innovation
Hellenic Republic (Greece)

University of Chicago, January 2021–June 2021
Academic Leave (Sabbatical)
Department of Computer Science
Physical Sciences Division

Carnegie Mellon University, 2003–2009
Research and Teaching Assistant
Department of Computer Science

Hewlett-Packard, 2002–2003
Senior System/Software Engineer
High Performance Servers Division

Compaq Computer Corporation, 1999–2001
Senior System/Software Engineer
Business Critical Systems

Digital Equipment Corporation, 1998
Senior System/Software Engineer
AlphaServer Product Development

Digital Equipment Corporation, 1997
Research Intern
Cambridge Research Lab

University of Rochester, 1995–1997
Research & Teaching Assistant
Department of Computer Science

EDUCATION

Carnegie Mellon University, Pittsburgh, PA, Ph.D. in Computer Science, July 2009
Thesis: *Chip-Multiprocessors for Server Workloads*
Committee: Babak Falsafi, Anastasia Ailamaki, David O'Hallaron, Todd C. Mowry, Luiz A. Barroso
Carnegie Mellon University, Pittsburgh, PA, M.S. in Computer Science, May 2006
University of Rochester, Rochester, NY, M.S. in Computer Science, May 1997
University of Crete, Heraklion, Crete, Greece, B.S. in Computer Science, September 1995

AWARDS AND HONORS

Future CRA Leader, Computing Research Association, 2024
Northwestern Academic Year Undergraduate Research Award, *Nikola Maruszewski* (adv. Nikos Hardavellas), Northwestern University, 2023
"A Compiler for Quantum Chiplets"
McCormick Summer Undergraduate Research Award, *Nikola Maruszewski* (adv. Nikos Hardavellas), Northwestern University, 2023
"A Compiler for Quantum Chiplets"
IEEE Micro Top Picks Honorable Mention, 2023
"SupermarQ: A Scalable Quantum Benchmark Suite"
The IEEE MICRO Top Picks award recognizes the year's most significant research papers in computer architecture based on novelty and long-term impact. It is given to 12 papers across all top publications in computer architecture (regardless of venue) throughout the entire calendar year, with the next 12 papers in the ranking receiving an honorable mention, corresponding to the top 1% of all submitted papers.
Associated Student Government Faculty & Administrator Honor Roll, Northwestern University, 2021–2022
Nominated by the undergraduate student body for contributions to COMP_SCI 213: Introduction to Computer Systems.
Northwestern Canvas Hall of Fame, Nomination, Northwestern University, 2023
Faculty Service Award, Department of Computer Science, Northwestern University, 2022
Best Paper Award, 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Seoul, South Korea, 2022
"SupermarQ: A Scalable Quantum Benchmark Suite"
Best Paper Award Nomination, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2021
"Pho$: A Case for Shared Optical Cache Hierarchies"
Test-of-Time Award, International Conference on Extending Database Technology (EDBT), 2019
"Shore-MT: A Scalable Storage Manager for the Multicore Era", EDBT 2009
Best Ph.D. Dissertation Award in Computer Engineering, *Yigit Demir* (adv. Nikos Hardavellas*)*, Northwestern University, 2016
"High-Performance and Energy-Efficient Computer System Design Using Photonic Interconnects"
NSF CAREER Award, Division of Computing & Communication Foundations (CCF), Directorate for Computer and Information Science and Engineering (CISE), National Science Foundation (NSF), 2015
"Energy-Efficient and Energy-Proportional Silicon-Photonic Manycore Architectures"
Interview, IEEE Computer, October 2013
"The Impact of Dynamic Directories on Multicore Interconnects", IEEE Computer Special Issue on Multi-core Memory Coherence, October 2013
IEEE Micro Spotlight Paper, February 2012
"Toward Dark Silicon in Servers", IEEE Micro Special Issue on Big Chips, July/August 2011
Fellow, Searle Center for Teaching Excellence, Northwestern University, 2012

Keynote Talk. 9th International Symposium on Parallel and Distributed Computing (ISPDC), 2010
"When Core Multiplicity Doesn't Add Up"
IEEE Micro Top Picks, 2010
"Near-Optimal Cache Block Placement with Reactive Nonuniform Cache Architectures"
The IEEE MICRO Top Picks award recognizes the year's most significant research papers in computer architecture based on novelty and long-term impact. It is given to 12 papers across all top publications in computer architecture (regardless of venue) throughout the entire calendar year, with the next 12 papers in the ranking receiving an honorable mention, corresponding to the top 1% of all submitted papers.
June and Donald Brewer Chair, Northwestern University, 2009–2011
Best Demonstration Award, IEEE International Conference on Data Engineering (ICDE), 2006
"Simultaneous Pipelining in QPipe: Exploiting Work Sharing Opportunities Across Queries"
Technical Award for Contributions to the Alpha Microprocessor, Compaq Computer Corporation, 2000
FORTH Fellowship, Foundation for Research and Technology-Hellas (FORTH), Greece, 1993–1995

PUBLICATIONS

Citations 4484 (Google Scholar), H-index 27, i10-index 46.

Peer-reviewed Conference Publications

1. "Pauli Check Sandwiching for Quantum Characterization and Error Mitigation during Runtime." Joshua Gao, Ji Liu, Alvin Gonzales, Zain H. Saleem, Nikos Hardavellas, Kaitlin N. Smith. IEEE International Conference on Quantum Computing and Engineering (**QCE**). (poster)
2. Pauli Check Extrapolation for Quantum Error Mitigation. Quinn Langfitt, Ji Liu, Benchen Huang, Alvin Gonzales, Kaitlin N. Smith, Nikos Hardavellas, and Zain H. Saleem. IEEE International Conference on Quantum Computing and Engineering (**QCE**). (poster)
3. "Generalized Collective Algorithms for the Exascale Era." Michael Wilkins, Hanming Wang, Peizhi Liu, Bangyen Pham, Yanfei Guo, Rajeev Thakur, Nikos Hardavellas and Peter Dinda. In Proceedings of the IEEE International Conference on Cluster Computing (**IEEE Cluster**), Santa Fe, New Mexico, November 2023 (acceptance rate 24%)
4. "WARDen: Specializing Cache Coherence for High-Level Parallel Languages." Michael Wilkins, Sam Westrick, Vijay Kandiah, Alex Bernat, Brian Suchy, Enrico Armenio Deiana, Simone Campanoni, Umut Acar, Peter Dinda and Nikos Hardavellas. In Proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization (**CGO**), Montreal, Canada, February 2023 (acceptance rate 36%)
5. "Parsimony: Enabling SIMD/Vector Programming in Standard Compiler Flows." Vijay Kandiah, Daniel Lustig, Oreste Villa, David Nellans and Nikos Hardavellas. In Proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization (**CGO**), Montreal, Canada, February 2023 (acceptance rate 36%)
6. "Program State Element Characterization." Enrico Armenio Deiana, Brian Suchy, Michael Wilkins, Brian Homerding, Tommy McMichen, Katarzyna Dunajewski, Peter Dinda, Nikos Hardavellas and Simone Campanoni. In Proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization (**CGO**), Montreal, Canada, February 2023 (acceptance rate 36%)
7. "ACCLAiM: Advancing the Practicality of MPI Collective Communication Autotuning Using Machine Learning." Michael Wilkins, Yanfei Guo, Rajeev Thakur, Peter Dinda and Nikos Hardavellas. In Proceedings of the IEEE International Conference on Cluster Computing (**IEEE Cluster**), Heidelberg, Germany, September 2022 (acceptance rate 24%)
8. "Computing With an All-Optical Cache Hierarchy Using Optical Phase Change Memory as Last Level Cache." Haiyang Han, Theoni Alexoudi, Chris Vagionas, Nikos Pleros and Nikos Hardavellas. In

Proceedings of the European Conference on Optical Communication (**ECOC**), Basel, Switzerland, September 2022 (poster)

9. "CARAT CAKE: Replacing Paging via Compiler/Kernel Cooperation." Brian Suchy, Souradip Ghosh, Aaron Nelson, Zhen Huang, Drew Kersnar, Siyuan Chai, Michael Cuevas, Alex Bernat, Gaurav Chaudhary, Nikos Hardavellas, Simone Campanoni, and Peter Dinda. In Proceedings of the 2022 Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), Lausanne, Switzerland, March 2022 (acceptance rate 20%)
10. "SupermarQ: A Scalable Quantum Benchmark Suite ." T. Tomesh, P. Gokhale, V. Omole, G. Ravi, K. Smith, J. Viszlai, X. Wu, N. Hardavellas, M. Martonosi, F. Chong. In Proceedings of the 28th IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), Seoul, South Korea, February 2022 (acceptance rate 30%) **(Best Paper Award) (IEEE Micro Top Picks Honorable Mention)**
11. "ST^2 GPU: An Energy-Efficient GPU Design with Spatio-Temporal Shared-Thread Speculative Adders." V. Kandiah, A.M. Gok, G. Tziantzioulis and N. Hardavellas. In Proceedings of the 2021 Design Automation Conference (**DAC**), San Francisco, CA, December 2021 (acceptance rate 23%)
12. "AccelWattch: A Power Modeling Framework for Modern GPUs." V. Kandiah, S. Peverelle, M. Khairy, J. Pan, A. Manjunath, T. G. Rogers, T. M. Aamodt and N. Hardavellas. In Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Athens, Greece, October 2021 (acceptance rate 22%)
13. "Pho$: A Case for Shared Optical Cache Hierarchies." H. Han, T. Alexoudi, C. Vagionas, N. Pleros and N. Hardavellas. In Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (**ISLPED**), July 2021 (acceptance rate 26%) **(Best Paper Award Nomination)**
14. "Task Parallel Assembly Language for Uncompromising Parallelism." M. Rainey, P. Dinda, K. Hale, R. Newton, U. A. Acar, N. Hardavellas, S. Campanoni. In Proceedings of the 42nd ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), June 2021 (acceptance rate 27%)
15. "CARAT: A Case for Virtual Memory through Compiler- and Runtime-based Address Translation." B. Suchy, S. Campanoni, N. Hardavellas and P. Dinda. In Proceedings of the 41st ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), London, UK, June 2020 (acceptance rate 22%)
16. "Prospects for Functional Address Translation." C. Hetland, G. Tziantzioulis, B. Suchy, K. Hale, N. Hardavellas and P. Dinda. In Proceedings of the 27th IEEE International Symposium on the Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (**MASCOTS**), Rennes, France, October 2019
17. "Paths to Fast Barrier Synchronization on the Node." C. Hetland, G. Tziantzioulis, B. Suchy, M. Leonard, J. Han, J. Albers, N. Hardavellas and P. Dinda. In Proceedings of the 28th International Symposium on High-Performance Parallel and Distributed Computing (**HPDC**), Phoenix, Arizona, June 2019 (acceptance rate 20%)
18. "Unconventional Parallelization of Nondeterministic Applications." E. A. Deiana, V. St-Amour, P. Dinda, N. Hardavellas and S. Campanoni. In Proceedings of the 23rd ACM International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), Williamsburg, VA, March 2018 (acceptance rate 17%)
19. "POSTER: The Liberation Day of Nondeterministic Programs." E. A. Deiana, V. St-Amour, P. Dinda, N. Hardavellas and S. Campanoni. In Proceedings of the 26th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), Portland, OR, September 2017 (acceptance rate 23% for full papers, 29% for posters)
20. "Harnessing Path Divergence for Laser Control in Data Center Networks." Y. Demir, N. Terzenidis, H. Han, D. Syrivelis, G. T. Kanellos, N. Hardavellas, N. Pleros, S. Kandula, and F. Bustamante. In Proceedings of the 2017 IEEE Photonics Society Summer Topical Meeting Series (**IEEE SUM**), Optical Switching

Technologies for Datacom and Computercom Applications (OSDC), San Juan, Puerto Rico, July 2017 **(Invited Paper)**

21. "VaLHALLA: Variable Latency History Aware Local-carry Lazy Adder." A. M. Gök and N. Hardavellas. In Proceedings of the 27th ACM Great Lakes Symposium on VLSI (**GLSVLSI**), Banff, Alberta, Canada, May 2017 (acceptance rate 24%)
22. "Energy Proportional Photonic Interconnects." Y. Demir and N. Hardavellas. In 12th International Conference on High Performance and Embedded Architectures and Compilers (**HiPEAC**), Stockholm, Sweden, January 2017
23. "Evaluation of K-Means Data Clustering Algorithm on Intel Xeon Phi." S. Lee, W.-k. Liao, A. Agrawal, N. Hardavellas and A. Choudhary. IEEE Conference on Big Data (**IEEE BigData**), pp. 2251–2260, Washington, D.C., December 2016 (acceptance rate 17%)
24. "SLaC: Stage Laser Control for a Flattened Butterfly Network." Y. Demir and N. Hardavellas. In Proceedings of the 22nd IEEE International Symposium on High Performance Computer Architecture (**HPCA**), Barcelona, Spain, March 2016 (acceptance rate 22%)
25. "Lazy Pipelines: Enhancing Quality in Approximate Computing." G. Tziantzioulis, A. M. Gök, S. M. Faisal, N. Hardavellas, S. Ogrenci-Memik, and S. Parthasarathy. In Proceedings of the Design, Automation, and Test in Europe (**DATE**), Dresden, Germany, March 2016 (acceptance rate 24%)
26. "Edge Importance Identification for Energy Efficient Graph Processing." S. M. Faisal, G. Tziantzioulis, A. M. Gök, S. Parthasarathy, N. Hardavellas, and S. Ogrenci-Memik. In Proceedings of the 2015 IEEE International Conference on Big Data (**IEEE BigData**), Santa Clara, CA, October 2015 (acceptance rate 18%)
27. "SCP: Synergistic Cache Compression and Prefetching." B. Patel, G. Memik and N. Hardavellas. In Proceedings of the 33rd IEEE International Conference on Computer Design (**ICCD**), New York City, NY, October 2015 (acceptance rate 31%)
28. "Parka: Thermally Insulated Nanophotonic Interconnects." Y. Demir and N. Hardavellas. In Proceedings of the 9th International Symposium on Networks-on-Chip (**NOCS**), Vancouver, Canada, September 2015 (acceptance rate 25%)
29. "b-HiVE: A Bit-Level History-Based Error Model with Value Correlation for Voltage-Scaled Integer and Floating Point Units." G. Tziantzioulis, A. M. Gök, S. M. Faisal, N. Hardavellas, S. Memik, and S. Parthasarathy. In Proceedings of the Design Automation Conference (**DAC**), San Francisco, CA, June 2015 (acceptance rate 18%)
30. "Towards Energy-Efficient Photonic Interconnects." Y. Demir and N. Hardavellas. In **Proceedings of SPIE**, Vol. 9368, Optical Interconnects XV, pp. 93680T – 93680T-12, San Francisco, CA, February 2015. Also selected to appear in **2015 SPIE Green Photonics, SPIE Photonics West**.
31. "LaC: Integrating Laser Control in a Photonic Interconnect." Y. Demir and N. Hardavellas. In Proceedings of the IEEE Photonics Conference (**IPC**), pp. 28–29, La Jolla, CA, October 2014
32. "EcoLaser: An Adaptive Laser Control for Energy-Efficient On-Chip Photonic Interconnects." Y. Demir and N. Hardavellas. In Proceedings of the International Symposium on Low Power Electronics and Design (**ISLPED**), pp. 3–8, La Jolla, CA, August 2014 (acceptance rate 23%)
33. "Galaxy: A High-Performance Energy-Efficient Multi-Chip Architecture Using Photonic Interconnects." Y. Demir, Y. Pan, S. Song, N. Hardavellas, G. Memik and J. Kim. In Proceedings of the ACM International Conference on Supercomputing (**ICS**), pp. 303–312, Munich, Germany, June 2014 (acceptance rate 20%)
34. "Dynamic Directories: Reducing On-Chip Interconnect Power in Multicores." A. Das, M. Schuchhardt, N. Hardavellas, G. Memik, and A. Choudhary. In Design, Automation, and Test in Europe (**DATE**), pp. 479–484, Dresden, Germany, March 2012 (acceptance rate 25%)
35. "Elastic Fidelity: Trading-Off Computational Accuracy for Energy Reduction." Sourya Roy, Tyler Clemons, S M Faisal, Ke Liu, Nikos Hardavellas and Srinivasan Parthasarathy. 16th International

Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), Newport Beach, California, March 2011 (poster)

36. "Hardware/Software Techniques for DRAM Thermal Management." S. Liu, B. Leung, A. Neckar, S. Ogrenci-Memik, G. Memik, and N. Hardavellas. In Proceedings of the 17th IEEE International Symposium on High Performance Computer Architecture (**HPCA**), pp. 515–525, San Antonio, TX, February 2011 (acceptance rate 18%)
37. "Data-Oriented Transaction Execution." I. Pandis, R. Johnson, N. Hardavellas and A. Ailamaki. In Proceedings of the 9th Hellenic Data Management Symposium (**HDMS**), Cyprus, July 2010
38. "Reactive NUCA: Near-Optimal Block Placement and Replication in Distributed Caches." N. Hardavellas, M. Ferdman, B. Falsafi and A. Ailamaki. In Proceedings of the 36th ACM/IEEE Annual International Symposium on Computer Architecture (**ISCA**), pp. 184–195, Austin, TX, June 2009 (acceptance rate 20%) **(IEEE Micro Top Picks Award)**
39. "Shore-MT: A Scalable Storage Manager for the Multicore Era." R. Johnson, I. Pandis, N. Hardavellas and A. Ailamaki. In Proceedings of the 12th International Conference on Extending Database Technology (**EDBT**), pp. 24–35, Saint-Petersburg, Russia, March 2009 (historic acceptance rate 19%) **(Test-of-Time Award)**
40. "To Share Or Not To Share?" R. Johnson, N. Hardavellas, I. Pandis, N. Mancheril, S. Harizopoulos, K. Sabirli, A. Ailamaki and B. Falsafi. In Proceedings of the 7th Hellenic Data Management Symposium (**HDMS**), Heraklion, Crete, Greece, July 2008
41. "Multi-bit Error Tolerant Caches Using Two-Dimensional Error Coding." J. Kim, N. Hardavellas, K. Mai, B. Falsafi and J. C. Hoe. In Proceedings of the 40th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), pp. 197–209, Chicago, IL, December 2007 (acceptance rate 21%)
42. "To Share Or Not To Share?" R. Johnson, N. Hardavellas, I. Pandis, N. Mancheril, S. Harizopoulos, K. Sabirli, A. Ailamaki and B. Falsafi. In Proceedings of the 33rd International Conference on Very Large Data Bases (**VLDB**), pp. 351–362, Vienna, Austria, September 2007 (acceptance rate 16%)
43. "An Analysis of Database System Performance on Chip Multiprocessors." N. Hardavellas, I. Pandis, R. Johnson, N. Mancheril, S. Harizopoulos, A. Ailamaki, B. Falsafi. In Proceedings of the 6th Hellenic Data Management Symposium (**HDMS**), Athens, Greece, July 2007
44. "Scheduling Threads for Constructive Cache Sharing on CMPs." S. Chen, P. B. Gibbons, M. Kozuch, V. Liaskovitis, A. Ailamaki, G. E. Blelloch, B. Falsafi, L. Fix, N. Hardavellas, T. C. Mowry and C. Wilkerson. In Proceedings of the 19th Annual ACM Symposium on Parallelism in Algorithms and Architectures (**SPAA**), pp. 105–115, San Diego, CA, June 2007
45. "Database Servers on Chip Multiprocessors: Limitations and Opportunities." N. Hardavellas, I. Pandis, R. Johnson, N. Mancheril, A. Ailamaki and B. Falsafi. In Proceedings of the 3rd Biennial Conference on Innovative Data Systems Research (**CIDR**), pp. 79–87, Asilomar, CA, January 2007
46. "Parallel Depth First vs. Work Stealing Schedulers on CMP Architectures." V. Liaskovitis, S. Chen, P. B. Gibbons, A. Ailamaki, G. E. Blelloch, B. Falsafi, L. Fix, N. Hardavellas, M. Kozuch, T. C. Mowry, C. Wilkerson. In Proceedings of the 18th Annual ACM International Symposium on Parallelism in Algorithms and Architectures (**SPAA**), pp. 330, Cambridge, MA, August 2006
47. "Simultaneous Pipelining in QPipe: Exploiting Work Sharing Opportunities Across Queries." D. Dash, K. Gao, N. Hardavellas, S. Harizopoulos, R. Johnson, N. Mancheril, I. Pandis, V. Shkapenyuk and A. Ailamaki. Demonstration. In Proceedings of the 22nd International Conference on Data Engineering (**ICDE**), Atlanta, GA, April 2006 (acceptance rate 19%) **(Best Demo Award)**
48. "Store-Ordered Streaming of Shared Memory." T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki and B. Falsafi. In Proceedings of the 14th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), pp. 75–86, Saint Louis, MO, September 2005 (acceptance rate 25%)

49. "Temporal Streaming of Shared Memory." T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, A. Ailamaki and B. Falsafi. In Proceedings of the 32nd ACM/IEEE Annual International Symposium on Computer Architecture (**ISCA**), pp. 222–233, Madison, WI, June 2005 (acceptance rate 23%)
50. "Cashmere-VLM: Remote Memory Paging for Software Distributed Shared Memory." S. Dwarkadas, N. Hardavellas, L. Kontothanassis, R. Nikhil and R. Stets. In Proceedings of the 13th IEEE/ACM International Parallel Processing Symposium (**IPPS**), pp. 153–159, San Juan, Puerto Rico, April 1999 (acceptance rate 43%)
51. "Cashmere-2L: Software Coherent Shared Memory on a Clustered Remote-Write Network." R. J. Stets, S. Dwarkadas, N. Hardavellas, G. C. Hunt, L. Kontothanassis, S. Parthasarathy and M. L. Scott. In Proceedings of the 16th ACM Symposium on Operating Systems Principles (**SOSP**), pp. 170–183, Saint-Malo, France, October 1997 (acceptance rate 17% – historic)
52. "VM-Based Shared Memory on Low-Latency, Remote-Memory-Access Networks." L. Kontothanassis, G. C. Hunt, R. J. Stets, N. Hardavellas, M. Cierniak, S. Parthasarathy, W. Meira Jr., S. Dwarkadas and M. L. Scott. In Proceedings of the 24th ACM/IEEE Annual International Symposium on Computer Architecture (**ISCA**), pp. 157–169, Denver, CO, June 1997 (acceptance rate 20%)
53. "Contention in Counting Networks." C. Busch, N. Hardavellas and M. Mavronicolas. In Proceedings of the 13th ACM Annual Symposium on Principles of Distributed Computing (**PODC**), Los Angeles, CA, August 1994 (historic acceptance rate 30%)
54. "Notes on Sorting and Counting Networks." N. Hardavellas, D. Karakos and M. Mavronicolas. In Proceedings of the 7th International Workshop on Distributed Algorithms (**WDAG**), Lecture Notes in Computer Science, Vol. 725/1993 (A. Schiper, ed.), Springer-Verlag, pp. 234–248, September 1993. The series was later renamed *The International Symposium on Distributed Computing* (**DISC**) (historic acceptance rate 24%)

Peer-reviewed Journal Articles

55. "A Practical Shared Optical Cache with Hybrid MWSR/R-SWMR NoC for Multicore Processors." Haiyang Han, Theoni Alexoudi, Chris Vagionas, Nikos Pleros and Nikos Hardavellas. In ACM Journal on Emerging Technologies in Computing Systems (**JETC**), 2022
56. "Temporal Approximate Function Memoization." G. Tziantzioulis, N. Hardavellas, S. Campanoni. In **IEEE Micro**, Special Issue on Approximate Computing, Vol. 38(4), July/August 2018
57. "Energy Proportional Photonic Interconnects." Y. Demir and N. Hardavellas. In ACM Transactions on Architecture and Code Optimization (**TACO**), Vol. 13(5), pp. 54:1–54:26, December 2016
58. "The Impact of Dynamic Directories on Multicore Interconnects." M. Schuchhardt, A. Das, N. Hardavellas, G. Memik, and A. Choudhary. In **IEEE Computer,** Special Issue on Multicore Memory Coherence, Vol. 46(10), pp. 32–39, October 2013
59. "The Rise and Fall of Dark Silicon." N. Hardavellas. In **USENIX ;login:**, Vol. 37(2), pp. 7–17, April 2012 **(Invited Paper)**
60. "Toward Dark Silicon in Servers." N. Hardavellas, M. Ferdman, B. Falsafi, and A. Ailamaki. In **IEEE Micro**, Special Issue on Big Chips, Vol. 31(4), pp. 6–15, July/August 2011 **(IEEE Micro Spotlight Paper)**
61. "Data-Oriented Transaction Execution." I. Pandis, R. Johnson, N. Hardavellas and A. Ailamaki. In Proceedings of the VLDB Endowment (**PVLDB**), Vol. 3(1), pp. 928–939, August 2010
62. "Near-Optimal Cache Block Placement with Reactive Nonuniform Cache Architectures." N. Hardavellas, M. Ferdman, B. Falsafi and A. Ailamaki. IEEE Micro, **Top Picks from Computer Architecture Conferences**, Vol. 30(1), pp. 20–28, January/February 2010
63. "SIMFLEX: a Fast, Accurate, Flexible Full-System Simulation Framework for Performance Evaluation of Server Architecture." N. Hardavellas, S. Somogyi, T. F. Wenisch, R. E. Wunderlich, S. Chen, J. Kim, B. Falsafi, J. C. Hoe, and A. Nowatzyk. In ACM **SIGMETRICS** Performance Evaluation Review (**PER**) Special Issue on Tools for Computer Architecture Research, Volume 31, Number 4, pp. 31–35, March 2004

64. "Efficient Use of Memory Mapped Interfaces for Shared Memory Computing." N. Hardavellas, G. C. Hunt, S. Ioannidis, R. J. Stets, S. Dwarkadas, L. Kontothanassis and M. L. Scott. In IEEE Technical Committee on Computer Architecture (**TCCA**) Special Issue on Distributed Shared Memory, pp. 28–33, March 1997

Books and Book Chapters

65. "Operator-Level Parallelism." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 2nd edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-1-4899-7993-3, Springer, 2018
66. "Execution Skew." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 2nd edition, L. Liu and M. T. Ozsu (Eds.), ISBN 978-1-4899-7993-3, Springer, 2018
67. "Inter-Query Parallelism." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 2nd edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-1-4899-7993-3, Springer, 2018
68. "Intra-Query Parallelism." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 2nd edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-1-4899-7993-3, Springer, 2018
69. "Stop-and-Go Operator." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 2nd edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-1-4899-7993-3, Springer, 2018
70. "Techniques for Energy Proportionality in Optical Interconnects." Y. Demir and N. Hardavellas. Photonic Interconnects for Computing Systems, Understanding and Pushing Design Challenges, M. Nikdast, G. Nicolescu, S. Le Beux, and J. Xu (Eds.), **River Publishers Series in Optics and Photonics**, ISBN 978-8-793-51980-0, eBook ISBN 978-8-793-51979-4, River Publishers, 2017
71. "Operator-Level Parallelism." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 1st edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-0-387-35544-3, eBook ISBN 978-0-387-39940-9, pp. 1981–1985, Springer, 2009
72. "Execution Skew." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 1st edition, L. Liu and M. T. Ozsu (Eds.), ISBN 978-0-387-35544-3, eBook ISBN 978-0-387-39940-9, pp. 1079, Springer, 2009
73. "Inter-Query Parallelism." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 1st edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-0-387-35544-3, eBook ISBN 978-0-387-39940-9, pp. 1566–1567, Springer, 2009
74. "Intra-Query Parallelism." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 1st edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-0-387-35544-3, eBook ISBN 978-0-387-39940-9, pp. 1567–1568, Springer, 2009
75. "Stop-and-Go Operator." N. Hardavellas and I. Pandis. **Encyclopedia of Database Systems**, 1st edition, L. Liu and M. T. Özsu (Eds.), ISBN 978-0-387-35544-3, eBook ISBN 978-0-387-39940-9, pp. 2794, Springer, 2009

Peer-reviewed Workshop Publications

76. "Evaluating Functional Memory-Managed Parallel Languages for HPC using the NAS Parallel Benchmarks." Michael Wilkins, Garrett Weil, Luke Arnold, Nikos Hardavellas and Peter Dinda. In the 28th International Workshop on High-Level Parallel Programming Models and Supportive Environments (**HIPS**), held in conjunction with the 37th IEEE International Parallel & Distributed Processing Symposium (**IPDPS**), St. Petersburg, Florida, May 2023
77. "A FACT-based Approach: Making ML Collective Autotuning Feasible on Exascale Systems." Michael Wilkins, Yanfei Guo, Rajeev Thakur, Nikos Hardavellas, Peter Dinda and Min Si. In the 2021 Workshop on Exascale MPI (**ExaMPI**), held in conjunction with Supercomputing 2021, the International Conference for High Performance Computing, Networking, Storage, and Analysis (**SC**), St. Louis, November 2021
78. "The Case for an Interwoven Parallel Hardware/Software Stack." K. Hale, S. Campanoni, N. Hardavellas and P. Dinda. In the 10th International Workshop on Runtime and Operating Systems for

Supercomputers (**ROSS**), held in conjunction with Supercomputing 2021, the International Conference for High Performance Computing, Networking, Storage, and Analysis (**SC**), St. Louis, November 2021

79. "Towards Energy-Proportional Photonic Interconnects." Y. Demir and N. Hardavellas. 2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (**OPTICS**), co-located with Design, Automation, and Test in Europe (**DATE**), Dresden, Germany, March 2016. **(Invited Paper)**
80. "Towards a Schlieren Camera." Bharath Pattabiraman, Robert Morton, Alexander Grabenhofer, Nikos Hardavellas, Jack Tumblin, and Venkatesh Gopal. In the 8th Annual Mid-West Graphics Workshop (**MIDGRAPH**), Chicago, IL, December 2012
81. "Load Balancing for Processing Spatio-Temporal Queries in Multi-Core Settings." A. Yaagoub, G. Trajcevski, P. Scheuermann, and N. Hardavellas. In the 11th International ACM Workshop on Data Engineering for Wireless and Mobile Access (**MobiDE**), co-located with the ACM SIGMOD International Conference on Management of Data and the ACM SIGMOD-SIGACT-SIGART Symposium on Principles of Database Systems (ACM SIGMOD/PODS), Scottsdale, AZ, May 2012
82. "Exploiting Dark Silicon for Energy Efficiency." Nikos Hardavellas. NSF Workshop on Sustainable Energy-Efficient Data Management (**SEEDM**), Arlington, VA, May 2011.
83. "Exploring Benefits and Designs of Optically-Connected Disintegrated Processor Architecture." Y. Pan, Y. Demir, N. Hardavellas, J. Kim and G. Memik. Workshop on the Interaction between Nanophotonic Devices and Systems (**WINDS**), co-located with the 43rd International Symposium on Microarchitecture (MICRO), Atlanta, GA, December 2010
84. "The Path Forward: Specialized Computing in the Datacenter." N. Hardavellas, M. Ferdman, A. Ailamaki and B. Falsafi. In the 2nd Workshop on Architectural Considerations for Large Datacenters (**ACLD**), co-located with the 37th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA), Saint-Malo, France, June 2010
85. "Memory Coherence Activity Prediction in Commercial Workloads." S. Somogyi, T. F. Wenisch, N. Hardavellas, J. Kim, A. Ailamaki and B. Falsafi. In the 3rd Workshop on Memory Performance Issues (**WMPI**), pp. 37–45, Munich, Germany, June 2004
86. "Software Cache Coherence with Memory Scaling." N. Hardavellas, L. Kontothanassis, R. Nikhil and R. J. Stets. In the 7th Workshop on Scalable Shared-Memory Multiprocessors (**SSMM**), Barcelona, Spain, June 1998
87. "Understanding the Performance of DSM Applications." W. Meira Jr., T. J. LeBlanc, N. Hardavellas and C. Amorim. Communication and Architectural Support for Network-Based Parallel Computing (**CANPC**), D. Panda and C. Stunkel Eds., Lecture Notes in Computer Science, Vol. 1199/1997, pp. 198–211, Springer Berlin/Heidelberg, February 1997, DOI: 10.1007/3-540-62573-9_15
88. "Implementation of Cashmere." M. L. Scott, W. Li, L. Kontothanassis, G. C. Hunt, M. Michael, R. J. Stets, N. Hardavellas, W. Meira Jr., A. Poulos, M. Cierniak, S. Parthasarathy and M. Zaki. In the 6th Workshop on Scalable Shared-Memory Multiprocessors (**SSMM**), Boston, MA, October 1996

Technical Reports and Preprints

89. "Pauli Check Sandwiching for Quantum Characterization and Error Mitigation during Runtime." Joshua Gao, Ji Liu, Alvin Gonzales, Zain H. Saleem, Nikos Hardavellas, Kaitlin N. Smith. arXiv Quantum Physics (quant-ph) arXiv:2408.05565, August 2024
90. "Pauli Check Extrapolation for Quantum Error Mitigation." Quinn Langfitt, Ji Liu, Benchen Huang, Alvin Gonzales, Kaitlin N. Smith, Nikos Hardavellas, and Zain H. Saleem. arXiv Quantum Physics (quant-ph) arXiv:2406.14759, June 2024
91. "SupermarQ: A Scalable Quantum Benchmark Suite." Teague Tomesh, Pranav Gokhale, Victory Omole, Gokul Subramanian Ravi, Kaitlin N. Smith, Joshua Viszlai, Xin-Chuan Wu, Nikos Hardavellas, Margaret R. Martonosi, and Frederic T. Chong. arXiv Quantum Physics (quant-ph); Hardware Architecture (cs.AR) preprint arXiv:2202.11045, February 2022

92. “Public Release and Validation of SPEC CPU2017 PinPoints.” Haiyang Han and Nikos Hardavellas. arXiv Performance (cs.PF); Hardware Architecture (cs.AR) preprint arXiv:2112.02083, December 2021
93. “Energy-Proportional Data Center Network Architecture Through OS, Switch and Laser Co-design.” Haiyang Han, Nikos Terzenidis, Dimitris Syrivelis, Arash F. Beldachi, George T. Kanellos, Yigit Demir, Jie Gu, Srikanth Kandula, Nikos Pleros, Fabián Bustamante, and Nikos Hardavellas. arXiv Networking and Internet Architecture (cs.NI); Hardware Architecture (cs.AR) preprint arXiv:2112.02083, December 2021
94. “LaC: Integrating Laser Control in a Photonic Interconnect.” Y. Demir and N. Hardavellas. Technical Report NU-EECS-14-03, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, April 2014
95. “EcoLaser: An Adaptive Laser Control for Energy Efficient On-Chip Photonic Interconnects.” Y. Demir and N. Hardavellas. Technical Report NU-EECS-14-02, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, April 2014
96. “Galaxy: A High-Performance Energy-Efficient Multi-Chip Architecture Using Photonic Interconnects.” Y. Demir, Y. Pan, S. Song, N. Hardavellas, J. Kim, and G. Memik. Technical Report NU-EECS-13-08, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, July 2013
97. “Elastic Fidelity: Trading-off Computational Accuracy for Energy Reduction.” S. Roy, T. Clemons, S. M. Faisal, K. Liu, N. Hardavellas, and S. Parthasarathy. Technical Report NWU-EECS-11-02, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, February 2011, arXiv Hardware Architecture (cs.AR) preprint arXiv:1111.4279, November 2011
98. “PAD: Power-Aware Directory Placement in Distributed Caches.” A. Das, M. Schuchhardt, N. Hardavellas, G. Memik and A. Choudhary. Technical Report NWU-EECS-10-11, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, December 2010
99. “Power Scaling: the Ultimate Obstacle to 1K-Core Chips.” N. Hardavellas, M. Ferdman, A. Ailamaki, B. Falsafi. Technical Report NWU-EECS-10-05, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, March 2010
100. “Data-Oriented Transaction Execution.” I. Pandis, R. Johnson, N. Hardavellas and A. Ailamaki. Technical Report CMU-CS-10-101, Computer Science Department, Carnegie Mellon University, Pittsburgh, PA, January 2010
101. “R-NUCA: Data Placement in Distributed Shared Caches.” N. Hardavellas, M. Ferdman, B. Falsafi and A. Ailamaki. Technical Report CALCM-TR-2008-001, Computer Architecture Lab, Carnegie Mellon University, Pittsburgh, PA, December 2008
102. “Shore-MT: A Quest for Scalability in the Many-Core Era.” R. Johnson, I. Pandis, N. Hardavellas and A. Ailamaki. Technical Report CMU-CS-08-114, Computer Science Department, Carnegie Mellon University, Pittsburgh, PA, April 2008
103. “An Analysis of Database System Performance on Chip Multiprocessors.” N. Hardavellas, I. Pandis, R. Johnson, N. Mancheril, S. Harizopoulos, A. Ailamaki and B. Falsafi. Technical Report CMU-CS-06-153, Computer Science Department, Carnegie Mellon University, Pittsburgh, PA, 2006
104. “SORDS: Just-In-Time Streaming of Temporally-Correlated Shared Data.” T. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki and B. Falsafi. Technical Report CALCM-TR-2004-002, Computer Architecture Lab, Carnegie Mellon University, Pittsburgh, PA, November 2004
105. “The Implementation of Cashmere.” R. J. Stets, D. Chen, S. Dwarkadas, N. Hardavellas, G. C. Hunt, L. Kontothanassis, G. Magklis, S. Parthasarathy, U. Rencuzogullari and M. L. Scott. Technical Report TR-723, Computer Science Department, University of Rochester, Rochester, NY, December 1999
106. “VM-Based Shared Memory on Low-Latency, Remote-Memory-Access Networks.” L. Kontothanassis, G. C. Hunt, R. J. Stets, N. Hardavellas, M. Cierniak, S. Parthasarathy, W. Meira Jr., S. Dwarkadas and M. L. Scott. Technical Report TR-643, Computer Science Department, University of Rochester, Rochester, NY, November 1996

107. "Notes on Sorting and Counting Networks." N. Hardavellas, D. Karakos and M. Mavronicolas. Technical Report FORTH-ICS/TR-092, Institute of Computer Science, Foundation for Research and Technology–Hellas, Crete, Greece, July 1993

Patents

108. "Adaptive Dirty-Block Purging." S. C. Steely Jr. and N. Hardavellas. U.S. patent 6,493,801. December 2002
109. "Apparatus and Method for Maintaining Data Coherence Within a Cluster of Symmetric Multiprocessors." L. I. Kontothanassis, M. L. Scott, N. Hardavellas, G. C. Hunt, R. J. Stets and S. Dwarkadas. U.S. patent 6,341,339. January 2002

Publicly Released Software and Datasets

Parsimony, a prototype of the Parsimony SPMD programming model for auto-vectorization implemented as an LLVM standalone compiler IR-to-IR pass that can work independently of other passes (2023)

CARMOT, an LLVM implementation of the Compiler and Runtime Memory Observation Tool for Program State Element Characterization. CARMOT provides programmers with recommendations on how to properly apply hard-to-reason-about abstractions such as transfer sets in OpenMP and C++ smart pointers (2023)

WARDen, a software implementation within Sniper and MPL of a cache coherence protocol that capitalizes on the WARD property of Parallel ML to drive cache coherence (2023)

SupermarQ, a scalable, hardware-agnostic quantum benchmark suite which uses application-level metrics to measure the performance of modern NISQ quantum computers (2021)

CARAT CAKE, an aerokernel (Nautilus) running with a CARAT address space abstraction implemented in LLVM. CARAT CAKE replaces paging in the kernel with a system that can operate using only physical addresses, with memory management delegated explicitly to the compiler with support by the runtime (2021)

SPEC2017 Pinballs, publicly distributed pinballs of SPEC CPU2017 SPECspeed benchmarks. The pinballs are collected for the *Sniper* architectural simulator and they are validated on CPI (2021)

AccelWattch, a microbenchmark-based quadratic programming optimization framework for the power modeling of modern GPUs, and an accurate power model for NVIDIA Quadro Volta GV100 (2021)

TPAL, a task-parallel assembly language for heartbeat scheduling that dramatically reduces the overheads of parallelism without compromising scalability (2021)

SoftInj, a software fault injection library that implements the b-HiVE error models (2015)

b-HiVE Hardware Characterization Dataset, a raw dataset of full-analog HSIM and SPICE simulations of industrial strength 64-bit integer ALUs, integer multipliers, bitwise logic operations, FP adders, FP multipliers, and FP dividers from OpenSparc T1 across voltage domains, along with controlled value correlation experiments (2015)

Shore-MT, a prototype scalable storage manager for the multicore era (2007)

Flexus, a scalable full-system cycle-accurate simulator of multicore and multiprocessor systems (2004)

MEDIA COVERAGE

Flipboard. Applying classical benchmarking methodologies to create a principled quantum benchmark suite | Amazon Web Services. March 16, 2022

AWS Quantum Computing Blog. Applying classical benchmarking methodologies to create a principled quantum benchmark suite. March 15, 2022

BSG. The Race to Quantum Advantage Depends on Benchmarking. February 23, 2022

Protivi, The Post-Quantum World PODCAST. Benchmarking Quantum Computers with Super.tech. March 9, 2022 (also available in **audible**, **Apple Podcasts**, **ivoox**, **Spreaker**, **Podcast Addict**)

EPiQC. Super.tech/EPiQC Research Informs New Suite of Benchmarks for Quantum Computers. February 28, 2022

The DeepTech Insider. Chicago-based Super.tech Releases SupermarQ – A New Suite of Benchmarks for Quantum Computers. February 27, 2022

ExBulletin. Super.tech Secures $1.65 Million Grant and Announces New Benchmark Auite for Quantum Computers. February 25, 2022

HPC wire. Super.tech Releases SupermarQ – A New Suite of Benchmarks for Quantum Computers. February 24, 2022

CB Insights, IonQ. Two New Quantum Benchmarking Suites Announced by IonQ and Super.Tech. February 24, 2022

The Quantum Observer. Chicago-based Super.tech Releases SupermarQ – A New Suite of Benchmarks for Quantum Computers. February 24, 2022

The Polsky Center for Entrepreneurship and Innovation, University of Chicago. Super.tech Secures $1.65M Grant and Launches New Benchmarking Suite for Quantum Computers. February 24, 2022

HESHMore. Chicago-based Super.tech Releases SupermarQ – A New Suite of Benchmarks for Quantum Computers. February 24, 2022

The Quantum Insider. Chicago-based Super.tech Releases SupermarQ – A New Suite of Benchmarks for Quantum Computers. February 24, 2022

Quantum Computing Report. Two New Quantum Benchmarking Suites Announced by IonQ and Super.Tech. February 23, 2022

Newsbreak. SupermarQ: A Scalable Quantum Benchmark Suite. February 22, 2022

Intel Developer Zone. Intel Parallel Computing Center at Northwestern University. December 19, 2014

MIT News. Smarter Caching. February 19, 2014

Computing Now. Software Engineering – The Impact of Dynamic Directories on Multicore Interconnects. October 9, 2013

IEEE Software. Srini Devadas speaks with author Nikos Hardavellas on The Impact of Dynamic Directories on Multicore Interconnects. October 4, 2013

RESEARCH GRANTS and GIFTS

Across institutions: $7,432,740; Northwestern portion: $4,798,086; Personal share: $2,214,013

1. AMD, Vivado ML Enterprise Edition, multi-seat floating license donation, 2023–24, $35,950
2. McCormick Summer Undergraduate Research Award, “A Compiler for Chiplet-Based Quantum Systems.” Nino Maruszewski (adv. Nikos Hardavellas), 2023, $4,500
3. Northwestern University Academic Year Undergraduate Research Grant, “A Compiler for Chiplet-Based Quantum Systems.” Nino Maruszewski (adv. Nikos Hardavellas), 2023, $1,000
4. McCormick Equipment Fund, “A Heterogeneous Hardware Testbed for Systems and Security Research.” Nikos Hardavellas (PI), Peter A. Dinda, S. Campanoni, Y. Chen, 2022, $75,000 (including $25,000 in CS Department supplemental funding)
5. NSF SPX-2119069, “Collaborative Research: PPoSS: LARGE: Unifying Software and Hardware to Achieve Performant and Scalable Frictionless Parallelism in the Heterogeneous Future.” Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, Umut Acar (CMU), Guy Blelloch (CMU), 2021–2025, $3,927,454 (NU portion: $1,927,455, personal share: $660,356)
    a. REU Supplement. Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2022, $16,000
    b. REU Supplement. Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2023, $16,000
    c. REU Supplement. Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2024, $16,000

6. Argonne National Laboratory subcontract, "Exploring Machine Learning-based Approaches to Auto-tuning Distributed Memory Communication", Peter A. Dinda and Nikos Hardavellas, 2021–2023, $449,636 (personal share: $221,208)
7. NSF SPX-2028851, "SPX: Collaborative Research: PPoSS: Planning: Unifying Software and Hardware to Achieve Performant and Scalable Zero-cost Parallelism in the Heterogeneous Future." Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, Umut Acar (CMU), Michael Rainey (CMU), Kyle C. Hale (IIT), 2020–2023, $275,420 (NU portion: $128,343, personal share: $42,631)
    a. REU Supplement. Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2021, $16,000
8. NSF CNS-1763743, "CSR: Medium: Collaborative Research: Interweaving the Parallel Software/Hardware Stack." Peter A. Dinda (PI), Simone Campanoni, Nikos Hardavellas, Kyle C. Hale (IIT), 2018–2023, $1,214,853 (NU portion: $909,275, personal share: $303,119)
    a. REU Supplement. Peter A. Dinda (PI), Simone Campanoni, Nikos Hardavellas, 2020, $16,000
    b. REU Supplement. Peter A. Dinda (PI), Simone Campanoni, Nikos Hardavellas, 2021, $16,000
    c. REU Supplement. Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2022, $16,000
9. NSF CCF-1453853, "CAREER: Energy-Efficient and Energy-Proportional Silicon-Photonic Manycore Architectures." Nikos Hardavellas (PI), 2015–2021, $470,000
10. Intel Parallel Computing Center, Nikos Hardavellas (EECS), Vadim Linetsky (IEMS, PI), Diego Klabjan (IEMS), Jeremy C. Staum (IEMS), 2015–2017, $380,000 (personal share: $95,000)
11. ISEN, Booster Award, "Toward Energy-Efficient Computing on Dark Silicon." Nikos Hardavellas (PI), 2013–2014, $37,658
12. NSF CCF-1218768, "SHF:Small:Collabroative Research: Elastic Fidelity: Trading-off Computational Accuracy for Energy Efficiency." Nikos Hardavellas (PI), Seda Ogrenci-Memik, Srinivasan Parthasarathy (OSU), 2012–2015, $399,999 (NU portion: $217,999, personal share: $199,738)
13. Allinea Performance Analysis Software License Donation, 2015–2016, estimated value $11,970
14. Cadence, Tensilica XTensa Processor Generator Software License Donation, 2013–2015
15. Mentor Graphics, FloTHERM/Icepack Software License Donation, 2012–2015, estimated value $37,300

SELECTED INVITED PRESENTATIONS

1. "Research at PARAG@N." National University of Athens, Athens, Greece, May 2023
2. "Research at PARAG@N." National Technical University of Athens, Athens, Greece, May 2023
3. "Energy-Proportional Photonic Interconnects: From the Chip to the Datacenter." IBM Research, T. J. Watson Research Center, Yorktown Heights, NY, USA, December 2018
4. "Harnessing Path Divergence for Laser Control in Data Center Networks." IEEE Photonics Society Summer Topical Meeting Series (**IEEE SUM**), Optical Switching Technologies for Datacom and Computercom Applications (OSDC), San Juan, Puerto Rico, July 2017
5. "Elastic Fidelity Computing Across Layers", Workshop on FPGAs for Scientific Simulation and Data Analytics, National Center for Supercomputing Applications, University of Illinois at Urbana-Champaign, Urbana, IL, October 2016
6. "Towards Energy-Proportional Photonic Interconnects." 2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (**OPTICS**), co-located with the Design, Automation, and Test in Europe (**DATE**), Dresden, Germany, March 2016
7. "Energy-Proportional Photonic Interconnects." School of Computer and Communication Sciences, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, September 2014
8. "Galaxy: A High-Performance Energy-Efficient Multi-Chip Architecture Using Photonic Interconnects." School of Computer and Communication Sciences, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, April 2014
9. "Galaxy: High-Performance Energy-Efficient Multi-Chip Architectures Using Photonic Interconnects." Intel VSSAD, Hudson, MA, USA, May 2013

10. "Galaxy: High-Performance Energy-Efficient Multi-Chip Architectures Using Photonic Interconnects." Google, Madison, WI, USA, March 2013
11. "How to Excel in Graduate School." 3rd CRA-W/CDC Computer Architecture Summer School, Discipline-specific Mentoring Workshops, Computing Research Association's Committee on the Status of Women (CRA-W) and the Coalition to Diversify Computing (CDC), Northwestern University, August 2012
12. "Toward Energy-Efficient Computing." IBM Research, T. J. Watson Research Center, Yorktown Heights, NY, USA, March 2012
13. "Toward Energy-Efficient Computing." Google, Chicago, IL, USA, March 2012
14. "Pushing Back the Power Wall." DARPA PERFECT Workshop, Arlington, VA, February 2011
15. "The Rise of Dark Silicon." 14th International Workshop on High Performance Transaction Systems (**HPTS**), Asilomar, CA, USA, October 2011
16. "Toward Energy-Efficient Computing." Intel Microprocessor Technology Lab, Santa Clara, CA, Oct. 2011
17. "Future Directions in Multicore Design." Intel Microprocessor Technology Lab, Santa Clara, CA, May 2011
18. "Exploiting Dark Silicon for Energy Efficiency." NSF Workshop on Sustainable Energy-Efficient Data Management (**SEEDM**), Arlington, VA, USA, May 2011
19. "Exploiting Dark Silicon in Server Design." Department of Computer Science, Illinois Institute of Technology, Chicago, IL, March 2011
20. "When Core Multiplicity Doesn't Add Up." **Keynote Talk**, 9th International Symposium on Parallel and Distributed Architectures (**ISPDC**), Istanbul, Turkey, July 2010
21. "Elastic Caches." Department of Informatics and Telecommunications, University of Athens, Greece, June 2010
22. "Near-Optimal Cache Block Placement with Reactive Nonuniform Cache Architectures." Department of Computer Architecture, Universitat Politècnica de Catalunya, Barcelona, Spain, March 2010
23. "Near-Optimal Block Placement and Replication in Distributed Caches." Department of Electrical Eng. and Computer Science, Northwestern University, March 2009
24. "Near-Optimal Block Placement and Replication in Distributed Caches." Department of Computer Science, Rutgers University, March 2009
25. "Near-Optimal Block Placement and Replication in Distributed Caches." Department of Electrical and Computer Eng., North Carolina State University, April 2009
26. "SIMFLEX and ProtoFlex: Fast, Accurate and Flexible Simulation of Computer Systems." **Tutorial**, 17th International Conference on Parallel Architecture and Compilation Techniques (**PACT**), Toronto, Canada, October 2008
27. "R-NUCA: Data Placement in Distributed Shared Caches." School of Computer and Communication Sciences, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, May 2008
28. "Multicore: friend… or foe? Multicore Architecture, Scalability." Invited Talk, Workshop on Concurrency, Department of Computer Science, Carnegie Mellon University, February 2008
29. "Database Servers on Chip Multiprocessors: Limitations and Opportunities." Parallel Data Lab (PDL) Retreat, Carnegie Mellon University, Nemacolin Woodlands Resort, PA, October 2006
30. "SORDS: Just-In-Time Streaming of Temporally Correlated Shared Data." Foundation for Research and Technology-Hellas (FORTH), Institute of Computer Science, Crete, Greece, June 2004
31. "VM-Based Shared Memory on Remote-Memory-Access Networks: the Cashmere Project." Microprocessor Research Lab, Intel Corporation, Portland, OR, August 1997

PROFESSIONAL SERVICE

Steering Committees

IEEE/ACM International Symposium on Microarchitecture (**MICRO**), 2023–
Greater Chicago Area Systems Research Workshop (**GCASR**), 2013–2020

Technical and External Program Committees

1. 52nd Annual International Symposium on Computer Architecture (**ISCA**), Tokyo, Japan, June 2025
2. 57th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Austin, TX, October 2024
3. 30th IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), Edinburgh, Scotland, February 2024
4. 50th Annual International Symposium on Computer Architecture (**ISCA**), Orlando, FL, June 2023 (external committee)
5. 29th IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), Montreal, Canada, February 2023
6. 49th Annual International Symposium on Computer Architecture (**ISCA**), New York, NY, June 2022
7. **IEEE Micro Top Picks 2022** Selection Committee, 2022
8. 28th IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), Seoul, South Korea, February 2022 (external committee)
9. 50th International Conference on Parallel Processing (**ICPP**), Argonne National Labs, IL, USA, August 2021
10. 48th Annual International Symposium on Computer Architecture (**ISCA**), Valencia, Spain, May 2021 (external committee)
11. 2021 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**), March 2021
12. 47th Annual International Symposium on Computer Architecture (**ISCA**), May 2020 (external committee)
13. 53rd Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), October 2020 (external committee)
14. 2020 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**), April 2020
15. 52nd Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Columbus, OH, October 2019 (external committee)
16. Workshop on Approximate Computing Across the Stack (**WAX**), co-located with the ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), Phoenix, Arizona, June 2019
17. 5th International Workshop on Optical/Photonic Interconnects for Computing Systems (**OPTICS**), co-located with the Design, Automation and Test in Europe (**DATE**), Florence, Italy, March 2019
18. 45th Annual International Symposium on Computer Architecture (**ISCA**), Los Angeles, CA, June 2018
19. 32nd IEEE International Parallel and Distributed Processing Symposium (**IPDPS**), Vancouver, BC, Canada, May 2018
20. 4th International Workshop on Optical/Photonic Interconnects for Computing Systems (**OPTICS**), co-located with the Design, Automation and Test in Europe (**DATE**), Dresden, Germany, March 2018
21. 24th IEEE International Symposium on High Performance Computer Architecture (**HPCA**), Vienna, Austria, February 2018 (external committee)
22. ACM Transactions on Architecture and Code Optimization and 13th International Conference on High-Performance and Embedded Architectures and Compilers (**ACM TACO/HiPEAC**), Board of Distinguished Reviewers, Manchester, UK, January 2018
23. 44th Annual International Symposium on Computer Architecture (**ISCA**), Toronto, ON, Canada, June 2017 (external committee)
24. 2017 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**), San Francisco, CA, April 2017

25. 3rd International Workshop on Optical/Photonic Interconnects for Computing Systems (**OPTICS**), co-located with the Design, Automation and Test in Europe (**DATE**), Lausanne, Switzerland, March 2017
26. 23rd IEEE International Symposium on High Performance Computer Architecture (**HPCA**), Austin, TX, February 2017
27. ACM Transactions on Architecture and Code Optimization and 12th International Conference on High-Performance and Embedded Architectures and Compilers (**ACM TACO/HiPEAC**), Board of Distinguished Reviewers, Stockholm, Sweden, January 2017
28. 34th IEEE International Conference on Computer Design (**ICCD**), Processor Architecture Track, Phoenix, AZ, October 2016
29. 49th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Taipei, Taiwan, October 2016 (external committee)
30. 43rd Annual International Symposium on Computer Architecture (**ISCA**), Seoul, South Korea, Jun. 2016
31. 2016 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**), Uppsala, Sweden, April 2016
32. 30th IEEE International Parallel & Distributed Processing Symposium (**IPDPS**), Computer Architecture Track, Chicago, IL, USA, May 2016
33. 22nd IEEE International Symposium on High Performance Computer Architecture (**HPCA**), Barcelona, Spain, March 12-16, 2016 (external committee)
34. ACM Transactions on Architecture and Code Optimization and 11th International Conference on High-Performance and Embedded Architectures and Compilers (**ACM TACO/HiPEAC**), Board of Distinguished Reviewers, Prague, Czech Republic, January 2016
35. 48th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Waikiki, Hawaii, December 2015 (external committee)
36. 42nd Annual International Symposium on Computer Architecture (**ISCA**), Portland, OR, June 2015 (external committee)
37. Design, Automation, and Test in Europe (**DATE**), Architecture and Microarchitecture Track, Grenoble, France, March 2015
38. ACM Transactions on Architecture and Code Optimization and 10th International Conference on High-Performance and Embedded Architectures and Compilers (**ACM TACO/HiPEAC**), Board of Distinguished Reviewers, Amsterdam, Netherlands, January 2015
39. Symposium on Energy and Resilience in Parallel Programming (**ERPP**), Edinburgh, Scotland, UK, September 3-4, 2015
40. 47th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Cambridge, UK, December 2014 (external committee)
41. 23rd International Conference on Parallel Architectures and Compilation Techniques (**PACT**), Edmonton, Alberta, Canada, August 2014 (external committee)
42. ACM International Conference on Supercomputing (**ICS**), Munich, Germany, June 2014 (external committee)
43. Design, Automation, and Test in Europe (**DATE**), Architecture and Microarchitecture Track, Dresden, Germany, March 2014
44. ACM Transactions on Architecture and Code Optimization and 9th International Conference on High-Performance and Embedded Architectures and Compilers (**ACM TACO/HiPEAC**), Board of Distinguished Reviewers, Vienna, Austria, January 2014
45. 13th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (**SAMOS XIII**), Applications, Systems, Architectures, and Processors Track, Samos, Greece, July 2013
46. Design, Automation, and Test in Europe (**DATE**), Architecture and Microarchitecture track, Grenoble, France, March 2013

47. ACM Transactions on Architecture and Code Optimization and 8th International Conference on High-Performance and Embedded Architectures and Compilers (**ACM TACO/HiPEAC**), Board of Distinguished Reviewers, Berlin, Germany, January 2013
48. 45th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Vancouver, BC, Canada, December 2012
49. IEEE International Symposium on Workload Characterization (**IISWC**), Austin, TX, November 2012. Also, member of the Best Paper subcommittee.
50. 1st Dark Silicon Workshop (**DaSi**), co-located with ISCA-2012, Portland, OR, June 2012
51. ACM SIGPLAN Workshop on Memory Systems Performance & Correctness (**MSPC**), co-located with PLDI-2012, Beijing, China, June 2012
52. 8th International Workshop on Data Management on New Hardware (**DaMoN**), Scottsdale, AZ, May 2012
53. 2012 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**), New Brunswick, NJ, April 2012
54. Design, Automation, and Test in Europe (**DATE**), Architectural and Micro-Architectural Design track, Dresden, Germany, March 2012
55. 44th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Porto Alegre, Brazil, December 2011
56. 29th IEEE International Conference on Computer Design (**ICCD**), University of Massachusetts, Amherst, October 2011
57. 10th IEEE International Symposium on Network Computing and Applications (**IEEE NCA**), Cambridge, MA, August 2011
58. 6th IEEE International Conference on Networking, Architecture, and Storage (**IEEE NAS**), Dalian, China, July 2011
59. Design, Automation, and Test in Europe (**DATE**), Architectural and Micro-Architectural Design Track, Grenoble, France, March 2011
60. 19th Euromicro International Conference on Parallel, Distributed and Network-Based Computing (**PDP**), special session on On-Chip Parallel and Network-Based Systems, Ayia Napa, Cyprus, Feb. 2011
61. 16th International Conference on the Management of Data (**COMAD**), Nagpur, Maharashtra, India, December 2010
62. 28th IEEE International Conference on Computer Design (**ICCD**), Computer Systems Design and Applications Track, Amsterdam, Netherlands, October 2010
63. 6th Annual Workshop on the Interaction between Operating Systems and Computer Architecture (**WIOSCA**), held in conjunction with ISCA-37, Saint-Malo, France, June 2010
64. Design, Automation, and Test in Europe (**DATE**), Architectural and Micro-Architectural Design Track, Dresden, Germany, March 2010

Conference and Workshop Session Chair

1. 12th International Conference on High Performance and Embedded Architectures and Compilers **(HiPEAC)**, Stockholm, Sweden, January 2017. Session Chair: **Memory Systems**
2. 30th IEEE International Parallel & Distributed Processing Symposium (**IPDPS**), Computer Architecture Track, Chicago, IL, May 2016. Session Chair, **Memory Management**
3. 5th Greater Chicago Area Systems Research Workshop (**GCASR**), Chicago, IL, April 2016. Session Chair, **GPU & Parallel Systems**
4. 33rd IEEE International Conference on Computer Design (**ICCD**), New York City, NY, October 2015. Session Chair, **Optimizations for Power and Speed**
5. 44th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Porto Alegre, Brazil, December 2011. Session Chair, **Compiler Support**

6. Design, Automation, and Test in Europe (**DATE**), Architectural and Micro-Architectural Design Track, Dresden, Germany, March 2010. Session Chair, **Innovative Memory Systems**

Conference and Workshop Organization

1. General co-Chair, 55th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**), Chicago, Illinois, 2022
2. Finance Chair, 30th IEEE International Conference on Data Engineering (**ICDE**), Chicago, Illinois, 2014
3. General and Program co-Chair, 2nd Greater Chicago-Area Systems Research Workshop (**GCASR**), Evanston, Illinois, 2013
4. Web Chair, 21st International Conference on Parallel Architectures and Compilation Techniques (**PACT**), Minneapolis, Minnesota, September 2012

Tutorials

"SIMFLEX and ProtoFlex: Fast, Accurate, and Flexible Simulation of Computer Systems." With M. Ferdman and E. Chung. 17th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), Toronto, Canada, October 2008

External Reviews

Reviewer for 30 conferences and 33 journal issues in computer architecture, parallel systems, compilers, embedded systems, VLSI, operating systems, databases, and theoretical computer science, including:
ISCA (2014–2010, 2006), MICRO (2013), HPCA (2014–2010), IEEE Transactions on VLSI (2018, 2015, 2011), IEEE Transactions on Computers (2020–2019, 2017–2015, 2013–2010), IEEE Transactions on Parallel and Distributed Systems (2016–2014), ACM Journal of Emerging Technologies in Computing Systems (2017), IEEE Micro (2013, 2012, 2010), IEEE Computer (2013), ISLPED (2012), IEEE Computer Architecture Letters (2015, 2014, 2012, 2009), ACM Transactions on Architecture and Code Optimization (2015–2013, 2010), Parallel Computing Journal (2015), ISPASS (2010, 2004), ISCAS (2010), DATE (2009), ASPLOS (2009, 2008), IPDPS (2009), Computing Frontiers (2008), VLDB (2007, 2006), Data and Knowledge Engineering Journal (2015, 2014), Journal on Theory of Computer Systems (2007), CASES (2007), GLSVLSI (2006), SIGMOD (2005), PACT (2005), ICS (2005), ICCAD (2003), HotOS (2001), Journal of Theoretical Computer Science (2001)

Funding Agencies Service

Domestic

NSF Grant Award Panelist/Reviewer: served on 18 panels organized by the divisions of Computer & Communication Foundations (**CCF**), Computer and Network Systems (**CNS**), and Information and Intelligent Systems (**IIS**), Directorate for Computer and Information Science and Engineering (**CISE**), **Expeditions** in Computing, and the Division of Electrical, Communications and Cyber Systems (**ECCS**), Directorate for Engineering (**ENG**), National Science Foundation (**NSF**), Arlington, VA, USA, and on panels in joint initiatives between NSF and the Semiconductor Research Corporation (**SRC**), and Intel, 2010–2024

DoE Grant Award Panelist/Reviewer, 2024

Invited Participant, Power Efficiency Revolution for Embedded Computing Technologies (**PERFECT**) Meeting, Microsystems Technology Office (MTO), Defense Advanced Research Projects Agency (**DARPA**), Arlington, VA, February 2012

Invited Delegate, NSF Workshop on Sustainable Energy-Efficient Data Management (**SEEDM**), Division of Information and Intelligent Systems (**IIS**), Directorate for Computer and Information Science and Engineering (**CISE**), National Science Foundation (**NSF**), Arlington, VA, May 2011

International

Reviewer, Academic Research Fund (AcRF) Tier 3, Singapore Ministry of Education, 2024

HFRI Grant Award Reviewer, Hellenic Foundation for Research & Innovation (**HFRI**), General Secretariat for Research and Innovation, Ministry of Development and Investments, Greece, 2023

NSERC Grant Award Reviewer, Natural Sciences and Engineering Research Council of Canada (**NSERC**), Manufacturing, Communications and Technologies Division, Canada, 2013

QNRF Grant award Reviewer, National Priorities Research Program, Qatar National Research Fund (**QNRF**), Qatar, 2016 and 2011

NSRF Grant Award Reviewer, Aristeia Research Program, National Strategic Reference Framework (**NSRF**), General Secretariat for Research and Technology, Ministry of Education, Greece, 2011

Outreach

Faculty Advisor (CS), Women's Quantum Computing Workshop, Northwestern University, Spring 2024

Faculty Advisor (CS), Student Seminar on Recent Quantum Advances, Northwestern University, Fall 2023–

Faculty Advisor (CS), Student's Quantum Computing Workshop, Northwestern University, Fall 2023

How to Design a Microprocessor, 11^{th}–12^{th} grade lesson module and graphical Mac/Windows application of a parameterized processor model that estimates the impact of design choices on performance, area, power, and off-chip data rates. The lesson addresses NGSS standards in Science and Engineering Practices (SEP), Disciplinary Core Ideas (DCI) HS-ETS1-2, 3, 4, and Cross Cutting Concepts, 2021

Invited Speaker, 3^{rd} CRA-W/CDC Computer Architecture Summer School, Discipline-specific Mentoring Workshops, Computing Research Association's Committee on the Status of Women (**CRA-W**) and the Coalition to Diversify Computing (**CDC**), Northwestern University, Evanston, IL, August 2012

School and University Service

McCormick Curriculum Committee, Northwestern University, 2019–2020

Google Ph.D. Fellowship Committee (4x), Northwestern University, 2016–2018, 2020, 2024

NSF CAREER Panel, Northwestern University, McCormick School of Engineering, 2016

Departmental Service

Served on 78 departmental committees at Northwestern and 1 at CMU—service counted separately per academic year

1. **Chair**, Faculty Search Committee, Computer Science and Electrical and Computer Engineering, Northwestern University, 2024–2025
2. Faculty Search Committee, Electrical and Computer Engineering – Division of Computer Engineering, Northwestern University, 2023–2024
3. Computing Infrastructure & NUIT/MCIT Liaison, Computer Science, Northwestern University, 2023-2024
4. Member, Reappointment, Tenure and Promotion Committee (3x), Computer Science, Northwestern University, 2019, 2024, 2025
5. **Chair**, Faculty Search Committee (2x), Computer Science, Northwestern University, 2021–2023
6. Strategy & Planning Committee (2x), Computer Science, Northwestern University, 2021–2023
7. **Chair**, Reappointment, Tenure and Promotion Committee (2x), Computer Science, Northwestern University, 2020, 2022
8. Faculty Search Committee, Electrical and Computer Engineering – Division of Solid State, Photonic, and Quantum Technologies, Northwestern University, 2021–2022
9. Faculty Search Committee (9x), Computer Science, Northwestern University, 2011–2020
10. **Director** of Graduate Studies (3x), Dept. of Electrical and Computer Engineering – Division of Computer Engineering, Northwestern University, 2018–2020

11. **Director** of Graduate Admissions (2x), Electrical and Computer Engineering – Division of Computer Engineering, Northwestern University, 2018–2020
12. Faculty Search Committee, Electrical Engineering and Computer Science – Division of Computer Engineering, Northwestern University, 2016–2017
13. Faculty Search Committee, Computer Science and the Segal Design Institute, Northwestern University, 2011–2012
14. Graduate Committee (13x), Electrical Engineering and Computer Science – Division of Computer Engineering, Northwestern University, 2009–2022
15. Undergraduate Curriculum Committee (13x), Electrical and Computer Engineering – Division of Computer Engineering, Northwestern University, 2009–2022
16. Distinguished Speakers Seminar Committee (3x), Electrical and Computer Engineering – Division of Computer Engineering, Northwestern University, 2015–2018
17. Computing Facilities Committee (13x), Electrical Engineering and Computer Science – Division of Computer Engineering, Northwestern University, 2009–2022
18. Security Warden (7x), Electrical Engineering and Computer Science – Division of Computer Engineering, Northwestern University, 2010–2017
19. Organizer, Computer Architecture Lab at Carnegie Mellon (CALCM) Seminar, CS, Carnegie Mellon, 2007

Ph.D. Thesis, Proposal, and Qualifying Exam Committees

1. Mike Wilkins, Ph.D. March 2024; Ph.D. Proposal April 2022 (**co-Chair**)
   Thesis: *On Transparent Optimizations for Communication in Highly Parallel Systems*
2. Yian Su, Qualifying Exam December 2023
3. Vijay Kandiah, Ph.D. November 2023; Ph.D. Proposal December 2022 (**Chair**)
   Thesis: *Uncovering Latent Hardware/Software Parallelism*
4. Enrico Deiana, Ph.D. November 2023; Ph.D. Proposal March 2020; Qualifying Exam February 2019
   Thesis: *Generating Thread-Level Parallelism in Nondeterministic Programs*
5. Nick Wanniger, Qualifying Exam May 2023
6. Griffin Dube, Qualifying Exam May 2023
7. Haiyang Han, Ph.D. May 2022; Ph.D. Proposal March 2020 (**Chair**)
   Thesis: *High-performance and Energy-efficient Computing Systems Using Photonics*
8. Brian Suchy, Ph.D. May 2022; Ph.D. Proposal July 2020; Qualifying Exam August 2019
   Thesis: *Revisiting Software-based Memory Management*
9. Panitan Wongse-ammat, Ph.D. Proposal April 2022
   Thesis: *RAT: Reconfigurable Address Translation*
10. Feng Lu, Ph.D. May 2020; Ph.D. Proposal January 2014
    Thesis: *Exploiting Program Locality for Efficient Online Fault Detection*
11. Majed Valad Beigi, Ph.D. August 2019; Ph.D. Proposal February 2017
    Thesis: *Thermal Optimizations for Emerging Technologies in 3D-Stacked High-Performance Chips*
12. Ali Murat Gök, Ph.D. December 2018, Ph.D. Proposal September 2016 (**Chair**)
    Thesis: *Energy-Efficient Computing through Approximate Arithmetic*
13. Yuanbo Fan, Ph.D. November 2018, Ph.D. Proposal January 2017
    Thesis: *Exploiting Circuit-Level Timing Slack for Energy Efficiency*
14. Chao Yan, Ph.D. Proposal September 2016, Ph.D. June 2018
    Thesis: *Behavior-Centric Fault Tolerant Caches to Enable Near-Threshold Voltage Scaling*
15. Conor Hetland, Qualifying Exam May 2018
16. Georgios Tziantzioulis, Ph.D. August 2017; Ph.D. Proposal October 2015 (**Chair**)
    Thesis: *Harnessing Approximation for Energy- and Power-Efficient Computing*

17. Dawei Li, Ph.D. May 2017, Ph.D. Proposal July 2015
    Thesis: *Integration of Thermocouple Technology into 3D IC for Thermal Management*
18. Kaicheng Zhang, Ph.D. April 2017, Ph.D. Proposal September 2015
    Thesis: *Thermal-aware Task Management for High Performance Systems*
19. Kyle C. Hale, Ph.D. August 2016; Ph.D. Proposal September 2014; Qualifying Exam March 2013
    Thesis: *Hybrid Runtime Systems*
20. Yigit Demir, Ph.D. August 2015 (**Chair**); Ph.D. Proposal September 2014 (**Chair**)
    Thesis: *High-Performance and Energy-Efficient Computer System Design Using Photonic Interconnects*
21. Giang Hoang, Ph.D. May 2014; Ph.D. Proposal April 2012
    Thesis: *Code Generation for Timing-Speculative Architectures*
22. Yuankai Chen, Ph.D. May 2014; Ph.D. Proposal May 2013
    Thesis: *Performance Optimization and Reliability Enhancement in High-Level Synthesis of VLSI Circuits*
23. Li Li, Ph.D. May 2014; Ph.D. Proposal May 2013
    Thesis: *Timing and Power Optimization for VLSI Design*
24. Anan Yaagoub, Ph.D. November 2013; Ph.D. Proposal October 2012
    Thesis: *Exploiting Domain Semantics for Efficient Parallelization of Spatial and Spatio-Temporal Queries*
25. Chang Bae, Ph.D. July 2013; Ph.D. Proposal June 2012
    Thesis: *Dynamic Adaptive Resource Management in a Virtual Machine Monitor for NUMA Multicore Systems*
26. Brian Leung, Ph.D. July 2012; Ph.D. Proposal December 2011
    Thesis: *Performance and Energy Optimizations for DRAM Memory Systems*
27. Jing Xin, Ph.D. March 2012; Ph.D. Proposal March 2011
    Thesis: *Exploring Instruction Level Timing Locality In Processor Pipelines*
28. Song Liu, Ph.D. June 2011
    Thesis: *Architectural and OS-Level Performance and Thermal Optimizations for DRAM Systems*
29. Yan Pan, Ph.D. March 2011
    Thesis: *Utilizing Nanophotonics in Future Many-core Processors*
30. Abhishek Das, Ph.D. October 2010; Ph.D. Proposal March 2010
    Thesis: *Micro-architectural Approaches for Power and Profitability in Multicore Processors*
31. Yu Zhang, Ph.D. June 2010; Ph.D. Proposal October 2009
    Thesis: *Adaptive On-Chip Networks and Their Impact on Processor Architectures*

M.S. Thesis and Project Exam Committees

1. Hanming Wang, M.S. November 2022 (**co-Chair**)
   Thesis: *Parameterization of MPI Collective Operation Algorithms for Autotuning*
2. Gaurav Chaudhary, M.S. December 2020 **(Chair)**
   Project: *A Simulator for Distributed Quantum Computing*
3. Benjamin Levinson, M.S. May 2019 **(Chair)**
   Thesis: *Address Translation Performance Modeling*
4. Sai Nikhil Bharadwaj Vishnubhatla, M.S. May 2018
   Project: *Study on Memristor-based Implementation of Hardware Accelerators*
5. Vijay Kandiah, M.S. December 2017 (**Chair)**
   Thesis: *The Impact of VaLHALLA Adders on GPUs*
6. Zhenduo Zhai, M.S. December 2017 (**Chair)**
   Project: *An Educational Tool for Multicore Design Space Analytic Modeling*
7. Matthew Arba Albrecht, M.S. May 2015
8. Fei Jia, M.S. December 2014

Thesis: *Multi-Speculative Adder*

9. Ajit Mukund Hunsur, M.S. November 2014
   Thesis: *Memory Mapping In Heterogeneous Multi-Core Architectures*
10. Besnik Pashaj, M.S. August 2014 (**Chair**)
    Thesis: *Performance and Power Analysis of Specialized Instruction Sets Processors*
11. Yixi Zhang, M.S. July 2013
    Thesis: *Generational Incremental Garbage Collectors*
12. Xinxin Huang, M.S. May 2013 (**Chair**)
    Project: *Modeling the Impact of Process and Thermal Variations and Materials on Nanophotonic Devices*
13. Bhargavraj Patel, M.S. May 2013 (**co-Chair**)
    Thesis: *Exploring a Compressed Cache to Implement Efficient Hardware Prefetching in Multicore Processors*
14. Ke Liu, M.S. December 2012 (**Chair**)
    Thesis: *Hardware Error Rate Characterization with Below-nominal Supply Voltages*
15. Mathew Lowes, M.S. March 2011 (**Chair**)
    Thesis: *A Feature Selection Framework for Data Prefetching*

Undergraduate Honors Thesis Committees

1. Jerry Xu, B.S. May 2023
   Thesis: *Accelerated Journal Bearing Hydrodynamic Lubrication Simulation on CUDA*
2. Sourya Roy, B.S. June 2011 (**Chair**)
   Thesis: *Elastic Fidelity: Trading-off Computational Accuracy for Energy Reduction*

Professional Memberships

Member, Association for Computing Machinery (**ACM**)
- Member, Special Interest Group on Computer Architecture (**SIGARCH**)
- Member, Special Interest Group on Microarchitecture (**SIGMICRO**)

Member, Institute of Electrical and Electronic Engineers (**IEEE**)
- Member, IEEE Computer Society (**IEEE CS**)
- Member, IEEE Computer Society Technical Committee on Computer Architecture (**TCCA**)
- Member, IEEE Computer Society Technical Committee on Microprogramming and Microarchitecture (**TCuARCH**)
- Member, IEEE Quantum Community (**IEEEQuantum**)
- Member, IEEE Photonics Society

STUDENTS

Current Ph.D. Advisees

1. Jessica Jeng; Chookaszian Fellowship, Northwestern University, 2023–2024
2. Atmn Patel
3. Connor Selna

Current M.S. Advisees

1. Tyler Dempski (BS/MS), Computer Engineering
2. Michael Gavrincea (BS/MS), Computer Science
3. Nino Maruszewski (BS/MS), Computer Science; Northwestern University Academic Year Undergraduate Research Award, 2023; McCormick Summer Undergraduate Research Award, 2023

Current Undergraduate Advisees

1. Elijah Esparza, Computer Engineering
2. Josh Karpel, Computer Engineering

Alumni (Ph.D.)

1. Michael Wilkins (co-advised with Peter Dinda), Ph.D. March 2024
   Royal E. Cabell Fellowship, Northwestern University, 2019–2020
   Thesis: *On Transparent Optimizations for Communication in Highly Parallel Systems*
   First employment: **Cornelis Networks**
2. Vijay Kandiah, Ph.D. November 2023
   Thesis: *Uncovering Latent Hardware/Software Parallelism*
   First employment: **Nvidia**
3. Haiyang (Drake) Han, Ph.D. May 2022
   Royal E. Cabell Fellowship, Northwestern University, 2015–2016
   Terminal Year Fellowship, Northwestern University, 2022
   Thesis: *High-performance and Energy-efficient Computing Systems Using Photonics*
   First employment: **Apple**
4. Ali Murat Gök, Ph.D. December 2018
   Thesis: *Energy-Efficient Computing through Approximate Arithmetic*
   First employment: **Argonne National Laboratory, Mathematics and Computer Science Division**
   Current employment: **Cerebras**
5. Georgios Tziantzioulis, Ph.D. June 2017
   Terminal Year Fellowship, Northwestern University, 2017
   Thesis: *Harnessing Approximation for Energy- and Power-Efficient Computing*
   First employment: **Princeton University, Department of Electrical Engineering**
   Current employment: **AMD Research (Boston)**
6. Yigit Demir, Ph.D. August 2015
   Best Ph.D. Dissertation Award in Computer Engineering, Northwestern University, 2016
   Morrison Fellowship, Northwestern University, 2011
   Thesis: *High-Performance and Energy-Efficient Computer System Design Using Photonic Interconnects*
   First employment: **Intel, Computational Lithography Technology Group**
   Current employment: **Google**

Alumni (Thesis/Project M.S.)

1. Hanming Wang, M.S. December 2022
   Thesis: *Parameterization of MPI Collective Operation Algorithms for Autotuning*
   First employment: **Oracle**
2. Ujjwal sai Kotaru, M.S. March 2021
   Project: *Optimal Cache Placement Oracle*
   First employment: **Intel**
3. Gaurav Chaudhary, M.S., December 2020
   Project: *A Simulator for Distributed Quantum Computing*
   First employment: **Apple**
4. Benjamin Levinson, M.S., May 2019
   Thesis: *Address Translation Performance Modeling*
   First employment: **Intel (Hillsboro, Oregon)**

5. Vijay Kandiah, M.S., December 2017
   Thesis: *The Impact of VaLHALLA Adders on GPUs*
   First employment: **Northwestern University (Ph.D.)**
6. Zhenduo Zhai, M.S., December 2017
   Project: An Educational Tool for Multicore Design Space Analytic Modeling
   First employment: **University of Missouri (Ph.D.)**
7. Besnik Pashaj, M.S., August 2014
   Thesis: *Performance and Power Analysis of Specialized Instruction Sets Processors*
   First employment: **Silicon Micro Display Inc.**
8. Xinxin Huang, M.S., June 2013
   Project: *The Impact of Process, Thermal Variations and Materials on Waveguide Losses*
   First employment: **Northwestern University (Enterprise Systems)**
9. Bhargavraj Patel, M.S., June 2013
   Thesis: *Exploring a Compressed Cache to Implement Efficient Hardware Prefetching in Multicore Processors*
   First employment: **Qualcomm**
10. Ke Liu, M.S., December 2012
    Walter P. Murphy Fellowship, Northwestern University, 2010–2011 and Spring 2012
    Thesis: *Hardware Error Rate Characterization with Below-Nominal Supply Voltages*
    First employment: **Intel CCDO (Hillsboro, Oregon)**
11. Mathew Lowes, M.S., March 2011
    Nation Merit Scholarship, Northwestern University, 2006
    Thesis: *A Feature Selection Framework for Data Prefetching*
    First employment: **Intel (Austin, Texas)**

Alumni (Undergraduate Researchers)

12. Souradip Ghosh
    Project: *Fast In-pipeline Interrupts*
    First employment: **Carnegie Mellon University (Ph.D.)**
13. Dave Washington
    Project: *Cache Allocation and Replacement Oracle*
    First employment: **Google**
14. Dana Wilson, B.S. June 2014
    Project: *Design for Dark Silicon*
15. First employment: **Google**
    Marija Spaic, B.S. June 2013
    Project: *Design for Dark Silicon*
    First employment: **Peddinghaus Corporation**
16. Sourya Roy, B.S. June 2011
    Undergraduate Research Award, Northwestern University, March 2011
    Honors Thesis: *Elastic Fidelity: Trading-off Computational Accuracy for Energy Reduction*
    First employment: **Keystone Strategy**
    Current employment: **Google**
17. Eric Anger, B.S. June 2010
    Undergraduate Research Award, Northwestern University, March 2010
    Project: *Distributed Caches*
    First employment: **Georgia Tech (Ph.D.)**

TEACHING

Average CTEC instructor rating across all courses taught in the last three years: 5.04. Max CTEC scale is 6.00.

Catalog Courses – Last 3 Years

COMP_SCI 368/468 & COMP_ENG 368/468 Programming Massively Parallel Processors w/ CUDA (2012–)
CTECs of last three offerings: 5.41, 5.29, 5.25

COMP_SCI 213 Introduction to Computer Systems (2012–)
CTECs of last three offerings: 3.89, 3.89, 4.18

COMP_ENG 452 Advanced Computer Architecture I (2024–)
CTECs of last three offerings: 5.38

MLDS-413 Introduction to Databases and Information Retrieval (2017–)
CTECs of last three offerings: 5.00, 5.50, 5.40

COMP_ENG 456 Modern Topics in Computer Architecture (2010–11, 2013–2023)
CTECs of last three offerings: 6.00, 4.75, 5.60

Catalog Courses – Older Than 3 Years

ELEC_ENG 100 Electrons, Photons, and Bits: Adventures in Electrical and Computer Engineering (Week 7 microprocessor module, Spring 2013–2016, 2018)
CTECs of last three offerings: 5.38, 5.22, 4.00 (CTECs for the entire course)

COMP_SCI 317 Data Management and Information Processing (2018)
CTECs: 5.02

COMP_ENG 395/495 Advanced Compiler Hacking (2015)
CTECs: 6.00

COMP_ENG 361 Computer Architecture I (2010)
CTECs: 4.86

COMP_ENG 303 Advanced Digital Logic Design (2010–12)
CTECs: 4.50, 4.93, 3.95