# CURRICULUM VITAE ET STUDIORUM

Simone Campanoni

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## Personal Information

Birthdate: April 30th, 1981
Birthplace: Tradate, Italy
Italian and American nationality
Native language: Italian
Foreign language: English
Pronouns: he/him

## Current Positions

- Tenure-track assistant professor at the Computer Science department of Northwestern University.
- Curtesy appointment at the Electrical and Computer Engineering department of Northwestern University.
- Co-director of the Center for Deep Learning of Northwestern University.

## Biography

Simone Campanoni is a tenure-track assistant professor at the Computer Science department of Northwestern University. Simone's main research area is compilers, with special interest in its relation with computer architecture, runtime systems, operating systems, and programming languages. In more detail, Simone and his research group are passionate about understanding how the abstractions around and within compilers need to evolve for the post-Moore's Law Era. This goal often leads them to vertical specialization of the hardware/software stack. Simone started the HELIX research project at Harvard University in 2010 as a post-doc working with Profs. David Brooks and Gu-Yeon Wei. HELIX uses static and dynamic compilation, run-time optimization, and architecture specialization to extract coarse-grained parallelism for many-core architectures from complex "sequential" code. Simone received his Ph.D. degree with highest honors from Politecnico di Milano University in 2009. His dissertation discusses theoretical and practical performance implications of thread level parallelism. To this end, Simone designed and built a bytecode virtual machine optimized for commodity multicore platforms. Simone is the author of ILDJIT, a parallel compilation framework that includes static and dynamic compilers as well as a bytecode virtual machine. ILDJIT has been used in several academic and industrial research projects, including HELIX.

## Research Interests

### Mining Advantages in Randomized Code (MARC)

The application landscape is rapidly evolving including more often randomized algorithms. Current compilers ignore whether or not a program being compiled is randomized, leaving important opportunities unexplored. The MARC research project aims to identify and exploit such opportunities.

### Parallelizing Sequential Code

The multicore revolution in microprocessor architecture has left most programs behind. A program that maps easily to multicore architectures is the exception, not the rule. I am interested in showing multiple ways to parallelize the others (e.g., common, sequentially-designed programs) for modern and next-generation architectures.
The HELIX research project demonstrates the potential of leveraging low latency communication links among cores within a single chip to efficiently run parallelized code. The HELIX compiler demonstrates this potential on today's commodity processors by automatically speeding up sequential programs previously thought not to be parallelizable. The HELIX-RC compiler/architecture co-design highlights the benefits of including hardware support for a proactive, cache-based, low-latency core-to-core interconnect. Finally, HELIX-UP, shows the value of coupling the approximate computing paradigm with the parallelization performed by the HELIX compiler.

### Compiling for Resilient Architecture

Safety margins in conventional architectures are conservative to *always* avoid computational errors leading to energy inefficiencies. Resilient architectures squeeze these margins to save energy, correcting errors through costly rollback. Co-designed compilers can help resilient architectures to reduce their overhead by adapting the running code to their run-time characteristics.
For example, in our ALARM compiler, a resilient architecture propagates information about run-time rollback up to the co-designed compiler, which dynamically adapts the code to reduce the likelihood of further roll-back.

### The power of modern compilers for the hardware-software stack

Modern compilers are more powerful than what they are currently used for. This research direction shows how modern compilers create opportunities to reconsider the abstractions used between the layers of the hardware-software stack. Changing such abstractions generates important benefits compared to how we have been designing systems.

### Bytecode Virtual Machines

Virtual machines designed to execute bytecode programs are everywhere. The most successful and widely-adopted examples are Java and .NET. Browsers are virtual machines as well thanks to their ability to run programs written in multiple languages (e.g., JavaScript).
A bytecode virtual machine usually includes several components. Code generators, code optimizers, garbage collectors, execution engine, and profilers are the most common ones. Understanding interactions of these components allows them to be co-designed, which open interesting optimization opportunities. To enable these studies, we built the open source ILDJIT compilation framework.
An example of these optimizations is the dynamic look-ahead (DLA). In DLA, code generators and optimizers are driven by feedback coming from the execution engine to suppress dynamic compilation latency.

# Awards

## Research

"*Automatically Accelerating Non-Numerical Programs By Extracting Threads with an Architecture-Compiler Co-Design*"

Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks
Communication ACM Research Highlights, December 2017

**Research Highlights** 2017

"*Automatically Accelerating Non-Numerical Programs By Architecture-Compiler Co-Design*"
Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks
IEEE Micro's Top Picks Honorable Mention in Computer Architecture Conferences

**Top Picks Honorable mentions** 2015

"*HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs*"

Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks
HiPEAC award for the ISCA 2014 paper

**award** 2014

"*The HELIX Project: Overview and Directions*"

Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks
HiPEAC award for the DAC 2012 paper

**award** 2012

"*Metronome: Operating System Level Performance Management via Self-Adaptive Computing*"

Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto and Marco D. Santambrogio
HiPEAC award for the DAC 2012 paper

**award** 2012

"*Voltage Noise in Production Processors*"

Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks
IEEE Micro's Top Picks in Computer Architecture Conferences

**Top Picks** 2011

"*Dynamic Compilation and Parallelism: Theory and large scale experimentation*"

Simone Campanoni
Ph.D. with the highest honors. Politecnico di Milano, 3 March 2010.


**Highest honors**
2010

"*A parallel dynamic compiler for CIL bytecode*"

Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi
Best paper for the PhDay at Politecnico di Milano, 2008


**Best paper**
2008

## Teaching

"*Best Teacher Award of the EECS Department*"

Northwestern University


**Best teacher**
**2018**

# Publications

## International Conferences

"*Task Parallel Assembly Language for Uncompromising Parallelism*" **PLDI**
Mike Rainey, Peter Dinda, Kyle Hale, Ryan Newton, Umut A. Acar, Nikos Hardavellas, and Simone Campanoni 2021
In proceedings of the 42st Conference on Programming Language Design and Implementation, 2021
Acceptance rate: 27.1% (87/320)

"*CODE: Compiler-Based Neuron-Aware Ensemble Training*" **MLSys**
Ettore M. G. Trainiti, Thanapon Noraset, David Demeter, Doug Downey, and Simone Campanoni 2021
In proceedings of the Machine Learning and Systems conference. April 4-7, 2021

"*Compiler-based Timing For Extremely Fine-grain Preemptive Parallelism*" **SC**
Souradip Ghosh, Michael Cuevas, Simone Campanoni, Peter Dinda 2020
In proceedings of the Super Computing conference, Atlanta, USA. November 14-20, 2020
Acceptance rate: 22.3%

"*CARAT: A Case for Virtual Memory through Compiler- And Runtime-based Address Translation*" **PLDI**
Brian Suchy, Simone Campanoni, Nikos Hardavellas, Peter Dinda 2020
In proceedings of the 41st Conference on Programming Language Design and Implementation, London, United Kingdom. June 15-20, 2020
Acceptance rate: 22.5% (77/341)

"*SCAF: A Speculation-Aware Collaborative Dependence Analysis Framework*" **PLDI**
Sotiris Apostolakis, Ziyang Xu, Susan Tan, Greg Chan, Simone Campanoni, and David I. August 2020
In proceedings of the 41st Conference on Programming Language Design and Implementation, London, United Kingdom. June 15-20, 2020
Acceptance rate: 22.5% (77/341)
Awarded the available and reusable badges from the Artifact Evaluation Committee


"*Perspective: A Sensible Approach to Speculative Automatic Parallelization*" **ASPLOS**
Sotiris Apostolakis, Ziyang Xu, Greg Chan, Simone Campanoni, and David I. August 2020
In proceedings of the 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Lausanne, Switzerland. March 16-20, 2020
Acceptance rate: 18% (86/476)
Awarded the available and reusable badges from the Artifact Evaluation Committee


"*Introducing the Pseudorandom Value Generator Selection in the Compilation Toolchain*" **CGO**
Michael Leonard, Simone Campanoni 2020
In proceedings of the 17th International Symposium on Code Generation and Optimization, San Diego, California, USA. February 22-26, 2020
Acceptance rate: 27.3% (26/95)

"*Time Squeezing for Tiny Devices*" **ISCA**
Yuanbo Fan, Simone Campanoni, and Russ Joseph 2019
In proceedings of the 46th International Symposium on Computer Architecture, Phoenix, Arizona, USA, June 22-26, 2019
Acceptance rate: 16.9% (62/365)

"*Workload Characterization of Nondeterministic Programs Parallelized by STATS*" **ISPASS**
Enrico Armenio Deiana, and Simone Campanoni 2019
In proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software, Madison, Wisconsin, USA, March 24-26, 2019
Acceptance rate: 29.5% (26/88)

"*Compiler-guided instruction-level clock scheduling for timing speculative processors*" **DAC**
Yuanbo Fan, Tianyu Jia, Jie Gu, Simone Campanoni, and Russ Joseph 2018
In proceedings of the 55th Design Automation Conference, San Francisco, California, USA, June 24-28, 2018
Acceptance rate: 24.3% (168/691)

"*Unconventional Parallelization of Nondeterministic Applications*" **ASPLOS**
Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, and Simone Campanoni 2018
In proceedings of the 23rd ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Williamsburg, VA, USA, March 24-28, 2018
Acceptance rate: 17.5% (56/319)

"*Performance Implications of Transient Loop-Carried Data Dependences in Automatically Parallelized Loops*" **CC**
Niall Murphy, Timothy Jones, Robert Mullins and Simone Campanoni 2016
In proceedings of the 25th International Conference on Compiler Construction, Barcelona, Spain, March 17-18, 2016
Acceptance rate: 31.1% (24 research papers/77)

"*Power-Awareness and Smart-Resource Management in Embedded Computing Systems*" **CODES+ISSS**
Alessandro A. Nacci, Gianluca C. Durelli, Josue Pagan, Marina Zapater, Matteo Ferroni, Riccardo Cattaneo, Monica Vallejo, Simone Campanoni, Jose Ayala, Marco D. Santambrogio 2015
In proceedings of the 13th International Conference on Hardware/Software Codesign and System Synthesis, Amsterdam, Netherlands. October 4-9, 2015
Invited paper

"*HELIX-UP: Relaxing Program Semantics to Unleash Parallelization*" **CGO**
Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks 2015
In proceedings of the 12th International Symposium on Code Generation and Optimization, San Francisco, California, USA. February 7-11, 2015
Acceptance rate: 27.3% (24/88)
One of four papers nominated for the Best Paper Award by the Program Committee
Acceptance rate of nominated papers: 4.6% (4/88)

"*HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs*" **ISCA**
Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks 2014

In proceedings of the 41st International Symposium on Computer Architecture, Minneapolis, Minnesota, USA, June 14-18, 2014
Acceptance rate: 17.8% (46/258)

"*The HELIX Project: Overview and Directions*" **DAC**
Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks 2012
In proceedings of the 48th Design Automation Conference, San Francisco, California, USA, June 3-7, 2012
Invited paper

"*Metronome: Operating System Level Performance Management via Self-Adaptive Computing*" **DAC**
Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto and Marco D. Santambrogio 2012
In proceedings of the 48th Design Automation Conference (**DAC**), San Francisco, California, USA, June 3-7, 2012
Acceptance rate: 22.7% (168/741)

"*HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing*" **CGO**
Simone Campanoni, Timothy M. Jones, Glenn Holloway, Vijay Janapa Reddi, Gu-Yeon Wei and David Brooks 2012
In proceeding of 10th International Symposium on Code Generation and Optimization, San Jose, California, USA, March 31st - April 4th, 2012
Acceptance rate: 28.9% (26/90)

"*Voltage Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software-guided Thread Scheduling*" **MICRO**
Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks 2010
In proceedings of 43rd International Symposium on Microarchitecture (**MICRO**), Atlanta, Georgia, USA, December 4-8, 2010
Acceptance rate: 18.1% (45/248)

"*Software-Assisted Hardware Reliability: Abstracting Circuit-level Challenges to the Software Stack*" **DAC**
Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Michael D. Smith, Gu-Yeon Wei, and David Brooks 2009
In proceedings of IEEE 2009 46th International Conference on Design Automation Conference, San Francisco, July 26-31, 2009
Acceptance rate: 21.7% (148/682)

"*Traces of control-flow graphs*" **DLT**
Simone Campanoni and Stefano Crespi Reghizzi 2009
In proceedings of 13th International Conference on Developments in Language Theory, Stuttgart University, Germany, June 30 - July 3, 2009
Acceptance rate: 45.7% (32/70)

"*Dynamic Look Ahead Compilation: a technique to hide JIT compilation latencies in multicore environment*" **CC**
Simone Campanoni, Martino Sykora, Giovanni Agosta and Stefano Crespi Reghizzi 2009
In proceedings of 18th International Conference on Compiler Construction, York, United Kingdom, March 22-29, 2009
Acceptance rate: 25% (18/72)

"*Node-Level Optimization of Wireless Sensor Networks*" **WiCOM**
Simone Campanoni and William Fornaciari 2008
In proceedings of IEEE 2008 Wireless Communications, Networking and Mobile Computing, Dalian, China, October 12-14, 2008

"*Models and Tradeoffs in WSN System-Level Design*" **DSD**
Simone Campanoni and William Fornaciari 2008
In proceedings of IEEE 2008 International Conference on Digital System Design, Parma, Italy, September 3-5, 2008
Acceptance rate: 26%

"*Multi-level Design and Optimization of Wireless Sensor Networks*" **INSS**
Simone Campanoni and William Fornaciari 2008
In proceedings of IEEE 2008 International Conference on Networked Sensing Systems, Kanazawa, Japan, June 17-19, 2008

"*Ensuring Feasibility of Wireless Sensor Networks*" **ICCSC**
Simone Campanoni and William Fornaciari 2008
In proceedings of IEEE 2008 International Conference on Circuits and Systems for Communications, Shanghai, China, May 26-28, 2008

"*SWORDFISH: a Framework to Formally Design WSNs Capturing Events*" **SoftCOM**
Simone Campanoni and William Fornaciari 2007
In proceedings of IEEE 2007 International Conference on Software, Telecommunications and Computer Networks, Split-Dubrovnik, Croatia, September 27-29, 2007

## Magazines

- Georgios Tziantzioulis, Nikos Hardavellas and Simone Campanoni. "Temporal Approximate Function Memoization". **IEEE Micro** special issue on approximate computing, 9 August 2018. IEEE computer Society Digital Library. IEEE Computer Society.
- Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks. "Automatically Accelerating Non-Numerical Programs By Extracting Threads with an Architecture-Compiler Co-Design". Communication ACM Research Highlights (**CACM**), December 2017.
- Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks. "HELIX: Making the Extraction of Thread-Level Parallelism Mainstream". **IEEE Micro**, 12 June 2012. IEEE computer Society Digital Library. IEEE Computer Society.
- Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise in Production Processors". **IEEE Micro**'s Top Picks in Computer Architecture Conferences. Vol. 3, no. 1, 2011.

## International Journals

- Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Kim Hazelwood, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Eliminating Voltage Emergencies via Software-Guided Code Transformations".

ACM Transactions on Architecture and Code Optimization (**TACO**). Vol. 7, no. 2, 2010.

- Simone Campanoni, Giovanni Agosta, Stefano Crespi Reghizzi and Andrea Di Biagio. "A highly flexible, parallel virtual machine: design and experience of ILDJIT". Software: Practice and Experience (**SPE**). Vol. 40, no. 2, 2010.

## Books

- Simone Campanoni. "Guide to ILDJIT". Springer. 1st Edition. September 2011. ISBN: 978-1-4471-2193-0.

## Book Chapters

- Marcello Mura, Simone Campanoni, William Fornaciari, Mariagiovanna Sami. "Optimal Design of Wireless Sensor Networks". Chapter 19 of "Methodologies and Technologies for Networked Enterprises", in Lecture Notes in Computer Science, Vol. 7200, Anastasi, G.; Bellini, E.; Di Nitto, E.; Ghezzi, C.; Tanca, L.; Zimeo, E. (Eds.), 2012, ISBN 978-3-642-31738-5, July 2012.

## Short Papers

- Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, Simone Campanoni. "The Liberation Day of Nondeterministic Programs". 26th International Conference on Parallel Architectures and Compilation Techniques (**PACT**). Portland, Oregon, USA, September 9-13, 2017.

- Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "ILDJIT: a parallel dynamic compiler". In proceedings of 16th IFIP/IEEE International Conference on Very Large Scale Integration (**VLSI-SoC**), Rhodes Island, Greece, October 13-15, 2008.

## International Workshops

- Khalid Al-Hawaj, Simone Campanoni, Gu-Yeon Wei, David Brooks. "Unified Cache: A Case for Low-Latency Communication". 3rd International Workshop on Parallelism in Mobile Platforms (**PRISM**). Portland, OR, USA. June 13-17, 2015.

- Niall Murphy, Timothy M. Jones, Simone Campanoni, Robert Mullins. "Limits of Static Dependence Analysis for Automatic Parallelization". 18th International Workshop on Compilers for Parallel Computing (**CPC**). London, UK. January 7-9, 2015.

- Simone Campanoni, Svilen Kanev, Kevin Brownell, Gu-Yeon Wei and David Brooks. "Breaking Cyclic-Multithreading Parallelization with XML Parsing". 2nd International Workshop on Parallelism in Mobile Platforms (**PRISM**). Minneapolis, Minnesota, USA, June 14, 2014.

- Simone Campanoni and Luca Rocchini. "Static Memory Management within Bytecode Languages on Multicore Systems". In proceedings of Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (**CHANGE**). Newport Beach, California, March 6, 2011.

- Michele Tartara, Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "Parallelism and Retargetability in the ILDJIT Dynamic Compiler". 23th International Conference on Architecture of Computing Systems (**ARCS**). Hannover, Germany, February 22th, 2010.

- Michele Tartara, Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "Just-In-Time compilation on ARM processors". In proceedings of ACM 4th Workshop on the Implementation, Compilation, Optimization of Object-Oriented Languages, Programs and Systems (**ICOOOLPS**). Genova, Italy, July 6th, 2009.
- Vijay Janapa Reddi, Meeta S. Gupta, Krishna K. Rangan, Simone Campanoni, Glenn Holloway, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise: Why It's Bad, and What To Do About It". In proceedings of IEEE 2009 5th Workshop on Silicon Errors in Logic - System Effects (**SELSE**), Stanford University, March 24th and 25th, 2009.
- Stefano Crespi Reghizzi and Simone Campanoni. "Traces of control-flow graphs". ESF Workshop on Developments and New Tracks in Trace Theory, Cremona, Italy, 9-11 October 2008.

### Italian National Conferences

- Simone Campanoni, Michele Tartara, and Stefano Crespi Reghizzi. "ILDJIT: A parallel, free software and highly flexible Dynamic Compiler". IV Conferenza Italiana sul Software Libero. Cagliari, Italy, 11 - 12 June 2010.
- Michele Tartara, Stefano Crespi Reghizzi and Simone Campanoni. "Extending hammocks for parallelism detection". Italian Conference on Theoretical Computer Science (ICTCS). Camerino, Italy, 15 - 17 September 2010.
- Simone Campanoni. "Parallelism on compilation and execution". PhDay at Politecnico di Milano, Milan, Italy, June 24, 2009.
- Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". PhDay at Politecnico di Milano, Best paper, Milan, Italy, June 26, 2008.

### Posters

- Simone Campanoni. "The MARC compiler: Mining Advantages in non-deteRministic Code". ARM Summit. September 2019.
- Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, and Simone Campanoni. "Unconventional Parallelization of Nondeterministic Applications". The 7th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2018.
- Georgios Tziantzioulis, Nikos Hardavellas and Simone Campanoni. "Temporal Approximate Function Memoization". The 6th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2017.
- Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, Simone Campanoni. "Soft Dependences: Who They Are, Where to Find Them, and How to Satisfy Them". The 6th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2017.
- Georgios Tziantzioulis, Haiyang Han, Nikos Hardavellas, Simone Campanoni. "Temporal Output Memoization". The 5th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2016.
- Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks. "Relaxing Program Semantics to Unleash Parallelization". In the Center for Future Architectures Research (C-FAR). November 2014.
- Michael Lyons, Judson Porter, Yakun Sophia Shao, Simone Campanoni, David Brooks. "Architecture Design for Fine-grained Hardware Acceleration". In The Gigascale Systems Research Center(GSRC) Annual Symposium, September 2010.

- Simone Campanoni. "Dynamic Compilation and Parallelism. Theory and Large Scale Experimentation". PhDay at Politecnico di Milano, Milan, Italy, June 26, 2009.
- Simone Campanoni. "ILDJIT: Intermediate Language Distributed Just In Time". PhDay at Politecnico di Milano, Milan, Italy, June 24, 2009.

## Theses

1. Simone Campanoni. "Dynamic Compilation and Parallelism: Theory and large scale experimentation". PhD Dissertation, December 2009.

2. Simone Campanoni. "Intermediate Language Distributed Just In Time for the CIL Bytecode". Master Thesis, July 2006.

3. Simone Campanoni. "Ontology Packet Manager". Bachelor Thesis, July 2004.

## Technical Reports

4. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". SIGPLAN Notices, Volume 43, Number 4, April, 2008.

5. Simone Campanoni and William Fornaciari. "Design and optimization of Wireless Sensor Networks". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 17, Anno 2008.

6. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 3, Anno 2008.

7. Simone Campanoni and William Fornaciari. "Board-Level clustering of sensor network nodes". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 61, Anno 2007.

## Tutorials

1. "Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with the 12th ISPA Conference). Milan, Italy. August 29th, 2014. Full day tutorial.

2. "ILDJIT: Hands-On ILDJIT for Static and Dynamic Program Analysis and Transformation". Presented at International Symposium on Code Generation and Optimization (CGO), April 2012. Full day tutorial.

3. "ILDJIT: a Compilation Framework for Static and Dynamic Program Analysis and Optimization". Presented at the 44th International Symposium on Microarchitecture (MICRO), December, 2011. Full day tutorial.

4. "ILDJIT: a compilation framework for program introspection, optimization and micro-architectural design." Presented at High-Performance and Embedded Architectures and Compilers (HiPEAC), January 2011. Half day tutorial.

5. "ILDJIT Compiler Framework for Architecture Research". Presented at the 43rd International Symposium on Microarchitecture (MICRO), December 4th, 2010. Half day tutorial.

## US Patents

1. "Methods and apparatus for parallel processing". Simone Campanoni, Gu-Yeon Wei, David Brooks, Kevin Brownell, Svilen Kanev. Pending.

## Grant

**October 2020 – September 2021** National Science Foundation
Co-PI of "Collaborative Research: PPoSS: Planning: Unifying Software and Hardware to Achieve Performant and Scalable Zero-cost Parallelism in the Heterogeneous Future", NSF CCF-2028851.
This project is in collaboration with

- Prof. Peter Dinda (Northwestern University)
- Prof. Nikos Hardavellas (Northwestern University)
- Kyle Hale (Illinois Institute of Technology)
- Umut Acar (Carnegie Mellon University)

Amount: $128,343 for Northwestern University

**November 2019 – December 2020** ARM
This grant is related to the paralleilzing compiler research direction.
Amount: $40,000

**October 2019 – September 2022** National Science Foundation
PI of "SHF: Small: The Compiler-Architecture Solution to the Data Dependent, Circuit-Level Critical-Paths Variations", NSF CCF1908488.
This project is in collaboration with

- Prof. Russell Joseph (Northwestern University)

Amount: $499,741

**September 2018 – August 2021** National Science Foundation
Co-PI of "CSR: Medium: Collaborative Research: Interweaving the Parallel Software/Hardware Stack", NSF CNS1763743, $912,000. (Includes $12K in REU funds.)
This project is in collaboration with

- Prof. Peter Dinda (Northwestern University)
- Nikos Hardavellas (Northwestern University)
- Kyle Hale (Illinois Institute of Technology)

Amount: across the two institutions, the funded total is $1.25 Million

**January 2011 – December 2011** Microsoft Research
This is a grant with Prof. David Brooks.
Amount: $20,000

**December 2010 – March 2011** HiPEAC
This grant is related to ILDJIT.
Amount: €8,000

**January 2007 – December 2009** ST Microelectronics
This grant covered the expenses of my PhD studies.

**September 2001 – July 2006** Politecnico di Milano
University scholarship awarded by regional institute (competitive scholarship based on GPA, credit hours earned and financial need).

## Academic and Professional Service

### Program Chair

- Program Co-Chair with Martina Maggio and Antonio Fernández at the 13-th IEEE "International Symposium on Parallel and Distributed Processing with Applications" (ISPA). Helsinki, Finland. August 20-22, 2015.

  **Website** http://research.comnet.aalto.fi/ISPA2015

- Program Co-Chair with Martina Maggio at the 12-th IEEE "International Symposium on Parallel and Distributed Processing with Applications" (ISPA). Milan, Italy. August 25-29, 2014.

  **Website** http://ispa14.necst.it

- Program Co-Chair at the 2nd edition of the IEEE Workshop on "Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments", (co-located with DAC), San Francisco, USA, June 3, 2012.

  **Website** http://change.ws.dei.polimi.it

- Vice-chairs of the track "Embedded Software and Optimization" at the 10th edition of the IEEE/IFIP "International Conference on Embedded and Ubiquitous Computing". Paphos, Cyprus. October 3-5, 2012.

### Program Committee

- International Conference on Compiler Construction (CC). 2021.
- International Conference on Parallel Architectures and Compilation Techniques (PACT). 2020.
- International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES). 2020.
- International Conference on Parallel Processing (ICPP). 2020.
- International Symposium on Code Generation and Optimization (CGO). 2020, 2019, 2017, 2015.
- IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS). 2019.
- IEEE International Symposium on Workload Characterization (IISWC). 2018.
- International Symposium on Microarchitecture (MICRO). 2017.
- ACM International Conference on Computing Frontiers (CF). 2017.
- 14-th IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA). 2016.
- ACM International Conference on Computing Frontiers (CF). 2016.
- 3rd edition of the workshop Parallelism in Mobile Platformse (PRISM). 2015.
- DAC Workshop on Suite of Embedded Applications and Kernels (SEAK). 2014.
- 7th IEEE International Symposium on Embedded Multicore Systems-on-chip (MCSoC-13). 2013.
- 11th edition of the IEEE/IFIP International Conference on Embedded and Ubiquitous Computing. 2013.
- 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC). 2013.

- 6th IEEE International Symposium on Embedded Multicore Systems-on-chip (MCSoC). 2012.
- special session Self-adaptable and autonomic systems at the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC). 2012.
- 9th edition of the IEEE/IFIP International Conference on Embedded and Ubiquitous Computing. 2011.
- 1st edition of the IEEE Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE), (co-located with ASPLOS). 2011.
- 1st edition of the IEEE Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (2 PARMA), (co-located with ARCS). 2010.

### Financial Chair

- IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS). 2020.

### Special Session Organizer

- Organizer together with Donatella Sciuto. Special session "Power-awareness and resource management in mobile and IoT computing systems".
- Organizer together with Lamia Youseff. Special session "The Future of Operating Systems for Embedded Systems and Software (ESS)" at the 50th Design Automation Conference (DAC), Austin, Texas, USA.
- Session chair of the special session "The Future of Operating Systems for Embedded Systems and Software (ESS)" at the 50th Design Automation Conference (DAC), Austin, Texas, USA.

### Journal and Magazine Reviewer

- Reviewer of the ACM Transactions on Architecture and Code Optimization (TACO) 2019, 2017, 2015, 2014, 2013, 2012
- Reviewer of the Microprocessors and Microsystems journal, Elsevier 2017, 2016.
- Reviewer of the IEICE Transactions on Information and Systems 2017.
- Reviewer of the IEEE Computer Architecture Letters 2015.
- Reviewer of the journal Computer 2015.
- Reviewer of IEEE Embedded Systems Letters 2014.
- Reviewer of the journal "Mobile Networks and Applications" 2013.
- Reviewer for the following magazines: IEEE Micro 2012.

### Session Chair

- Session "Dynamic Languages" at International Symposium on Code Generation and Optimization (CGO), 2020.
- Session "Performance Modeling and Prediction" at International Symposium on Performance Analysis of Systems and Software (ISPASS), 2019.
- Session "Parallelism and Concurrency" at International Symposium on Code Generation and Optimization (CGO), 2015.

## Publicity Chair

- International Symposium on Code Generation and Optimization (CGO), 2017.

## External Reviewer

- ISCA 2020, 2019, 2017, 2016
- HPCA 2019, 2012
- ASPLOS 2017, 2011
- MICRO 2014, 2012
- CGO 2014, 2013
- PACT 2010
- ICS 2011
- CCNC
- IEEE Consumer Communications and Networking Conference

## Workshop

- Invited to attend NSF Workshop on Future Directions for Parallel and Distributed Computing (SPX), 2019

## PhD Thesis Committee

- Spencer Florence. Advisor: Robby Findler. Northwestern 2020.
- Yuanbo Fan. Advisor: Russ Joseph. Northwestern 2018.
- Ali-Murat Gok. Advisor: Nikos Hardavellas. Northwestern 2018.
- Zhengyang Qu. Advisor: Yan Chen. Northwestern 2017.
- Georgios Tziantzioulis. Advisor: Nikos Hardavellas. Northwestern 2017.

## PhD Prospectus Committee

- Xutong Chen. Advisor: Yan Chen. Northwestern 2019.
- Daniel Feltey. Advisor: Robby Findler. Northwestern 2018.
- Spencer Florence. Advisor: Robby Findler. Northwestern 2018.
- Xiang Pan. Advisor: Yan Chen. Northwestern 2017.
- Ali-Murat Gok. Advisor: Nikos Hardavellas. Northwestern 2016.
- Zhengyang Qu. Advisor: Yan Chen. Northwestern 2016.
- Georgios Tziantzioulis. Advisor: Nikos Hardavellas. Northwestern 2015.

## Master Thesis Committee

- Yian Su. Advisor: Simone Campanoni. Northwestern 2020.
- Qirui Luo. Advisor: Han Liu. Northwestern 2020.
- Jiayi Wang. Advisor: Han Liu. Northwestern 2020.

## Other Committees

- Judge for the Student Research Competition (SRC) of the International Symposium on Code Generation and Optimization (CGO), 2020, 2017.
- Chair for the Student Research Competition (SRC) of the International Symposium on Code Generation and Optimization (CGO), 2018.

## Talks

1. "Introducing the Pseudorandom Value Generator Selection in the Compilation Toolchain".
   Presented at
   - the 17th International Symposium on Code Generation and Optimization (**CGO**), 2020.
2. "Liberating Threads from Non-Numerical Programs with an Architecture-Compiler Co-Design".
   Presented at
   - the ARM Summmit. Austin, Texas, USA. September 15-19, 2019.
3. "Time Squeezing for Tiny Devices".
   Presented at
   - the 46th International Symposium on Computer Architecture (ISCA). Phoenix, Arizona, USA. June 22-26, 2019. This talk was done together with Russ Joseph.
4. "My teaching approach".
   Presented at
   - Northwestern University at the annual award cerimony. June 7th, 2019.
5. "Deep Neural Networks Meet Compiler Technology".
   Presented at
   - Northwestern University at the Deep Neural Network Lab Kickoff Meeting. 2018.
6. "Compilers for the Post-Moore's Law Era".
   Presented at
   - Northwestern University, CS 496. 2020.
   - Northwestern University, CS 496. 2019.
   - Politecnico di Milano. 2018.
7. "Parallelization in the multicore era".
   Presented at
   - The Greater Chicago Area Systems Research Workshop (GCASR). 2016.
   - University of Massachussets, Northwestern, Harvard, Politecnico di Milano. 2015.
8. "The HELIX Parallelizing Compiler to Efficiently Manage Resources". Presented at the 13th International Conference on Hardware/Software Codesign and System Synthesis (**CODES+ISSS**), Amsterdam, Netherlands. October 6, 2015.
9. "HELIX-UP: Relaxing Program Semantics to Unleash Parallelization". Presented at the 12th International Symposium on Code Generation and Optimization (CGO). San Francisco, California, USA. February 7-11, 2015.
10. "Accelerating Sequential Code with the HELIX Parallelizing Compiler". Presented at Google. Cambridge, USA. November 11th, 2014. Invited talk.
11. "Should Compiler Designers (Re-)Focus on Extracting Parallelism?". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with ISPA). Milan, Italy. August 25th, 2014. Invited talk.

12. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs". Presented at the 41st International Symposium on Computer Architecture (ISCA), Minneapolis, Minnesota, USA, June 16, 2014.

13. "Breaking Cyclic-Multithreading Parallelization with XML Parsing". Presented at the 2nd International Workshop on Parallelism in Mobile Platforms (PRISM). Minneapolis, Minnesota, USA, June 14, 2014.

14. "The HELIX Project: Goal, Status, and Potentials". Presented at ARM. Cambridge, UK. January 29th, 2014. Invited talk.

15. "Extract Parallelism from Sequential Code for Current Commodity Multicore Processor". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with the 50th Design Automation Conference, DAC). Austin, Texas, USA. June 2nd, 2013. Invited talk.

16. "The HELIX Project: Overview and Directions". Presented at the 48th Design Automation Conference (DAC). San Francisco, California, USA. June 5th, 2012.

17. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing". Presented at the 10th International Symposium on Code Generation and Optimization (CGO). San Jose, California, USA. April 2nd, 2012.

18. "HELIX: The Importance of Predictability". Presented at Princeton University - Princeton, USA. October 3, 2012. Invited talk.

19. "Static Memory Management within Bytecode Languages on Multicore Systems". Presented at the Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE). Newport Beach, California. March 6th, 2011.

20. "ILDJIT: A compilation framework for CIL bytecode". Presented at

    - Harvard University - Cambridge, USA. April 28, 2010.
    - Microsoft Research - Seattle, USA. March 22, 2010.

21. "Dynamic Compilation and Parallelism: Theory and large scale experimentation". Presented at the PhD dissertation. Milan, Italy. March, 2009.

22. "Parallelism on compilation and execution". PhDay at Politecnico di Milano. Milan, Italy. June 24th, 2009.

23. "Traces of control-flow graphs". Presented at 13th International Conference on Developments in Language Theory (DLT). Stuttgart University, Germany. June 30, 2009.

24. "Dynamic Look Ahead Compilation: a technique to hide JIT compilation latencies in multicore environment". Presented at 18th International Conference on Compiler Construction (CC). York, United Kingdom. March 24, 2009.

25. "A parallel dynamic compiler for CIL bytecode". Presented at PhDay at Politecnico di Milano. Milan, Italy. June 26th, 2008.

26. "Traces of control-flow graphs: a feasibility study of using trace theory for compilation". Presented at "Developments and New Tracks in Trace Theory" workshop, Cremona, Italy, October 11, 2008. Invited talk.

27. "Node-Level Optimization of Wireless Sensor Networks". Presented at IEEE 2008 Wireless Communications, Networking and Mobile Computing (WiCOM). Dalian, China. October 13, 2008.

28. “Models and Tradeoffs in WSN System-Level Design”. Presented at IEEE 2008 International Conference on Digital System Design (DSD). Parma, Italy. September 4, 2008.

29. “Multi-level Design and Optimization of Wireless Sensor Networks”. Presented at IEEE 2008 International Conference on Networked Sensing Systems (INSS). Kanazawa, Japan. June 18, 2008.

30. “Ensuring Feasibility of Wireless Sensor Networks”. Presented at IEEE 2008 International Conference on Circuits and Systems for Communications (ICCSC). Shanghai, China. May 27, 2008.

31. “ILDJIT: a parallel dynamic compiler”. Presented at 16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC). Rhodes Island, Greece. October 14, 2008.

32. “SWORDFISH: a Framework to Formally Design WSNs Capturing Events”. Presented at IEEE 2007 International Conference on Software, Telecommunications and Computer Networks (SoftCOM). Split-Dubrovnik, Croatia. September 27, 2007.

33. “Common Language Infrastructure (CLI)”. Presented at Linux Day - Varese, Italy. October 5, 2007. Invited talk.

34. “Intermediate Language Distributed Just In Time for the CIL Bytecode”. Presented at the master thesis. Milan, Italy. July, 2006.

35. “DotGNU”. Presented at Linux Day - Sesto Calende, Italy. October 8, 2006. Invited talk.

36. “Ontology Packet Manager”. Presented at the bachelor thesis. July, 2004.

## Teaching Experience

### Course Instructor

**Northwestern University** EECS 322 Compiler Construction.
Target: Undergraduate students.
Hours taught: 50.
Student evaluation (median rating of the instruction / median rating of the course):

- Winter 2018-2019: ongoing.
- Spring 2017-2018: 5.55 out of 6.
- Spring 2016-2017: 6 out of 6.
- Spring 2015-2016 with Prof. Robert Bruce Findler: 5.67 out of 6 / 5.6 out of 6

**Northwestern University** EECS 323 Code analysis and transformation.
Target: Undergraduate and master students.
Hours taught: 50.
Student evaluation (median rating of the instruction / median rating of the course):

- Spring 2018-2019: 6 out of 6 / 5 out of 6
- Fall 2017-2018: 6 out of 6 / 5 out of 6
- Fall 2016-2017: 6 out of 6 / 5 out of 6
- Fall 2015-2016: 5.6 out of 6 / 5.4 out of 6

**Northwestern University** EECS 397/497 Advanced Topics in Compilers.
Target: Ph.D. and master students.
Hours taught: 50.
Student evaluation (overall rating of the course):

- Fall 2019-2020: ongoing.
- Fall 2018-2019: 5.5 out of 6.
- Fall 2017-2018: 6 out of 6.

**Northwestern University** The programming language and compilers week of CS 101 Computer Science: Concepts, Philosophy, and Connections.
Target: Undergraduate students.
Hours taught: 2.

- Fall 2019-2020: not available
- Fall 2018-2019: not available
- Fall 2017-2018: not available
- Fall 2016-2017: not available
- Fall 2015-2016: not available

**Northwestern University** CS 496 Introduction to Graduate Studies.
Target: First year PhD students.
Hours taught: 1.

- Fall 2020-2021: not available
- Fall 2019-2020: not available

- Fall 2018-2019: not available

**Politecnico di Milano** Computer Science Parallelism Course: Parallelism in wonderland: are you ready to see how deep the rabbit hole goes?
Target: Ph.D. students.
Hours taught: 20.
Student evaluation:

- Spring 2014-2015 with Prof. Marco D. Santambrogio: not available.

**Harvard University** Computer Science 253r: Virtual Machines.
Target: Ph.D. students.
Hours taught: 50.
Student evaluation:

- Fall 2010-2011 with Prof. Vijay Janapa Reddi: not available.

## Teaching Assistance

**November 2008 – January 2009** Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.
Target: Master students.
Hours taught: 10

**November 2008 – January 2009** Formal languages and compilers course at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 10

**March 2008 – July 2008** Software engineering at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 60

**November 2007 – January 2008** Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.
Target: Master students.
Hours taught: 10

**November 2007 – January 2008** Formal languages and compilers course at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 10

**March 2007 – July 2007** Software engineering at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 60

**November 2006 – January 2007** Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.
Target: Master students.
Hours taught: 10

**October 2006 – January 2007** Informatica B laboratory at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 20

## Research Advising

### PhD students

**2016 - Current** Enrico Armenio Deiana

**2020 - Current** Katarzyna Dunajewski

**2020 - Current** Brian Homerding

**2020 - Current** Tommy McMichen

### Undergraduate and master students

**2019 - 2020** Zhenqing Hu

**2016 - 2020** Ettore Maria Giuseppe Trainiti

**2018 - 2020** Yian Su

**2018** Jordan Timmerman

**2018** Sasha Weiss

**2018** Nathan John Shelly

**2018** Angelo Matni

**2018** Michael Leonard

**2016** Shrivant Bhartia

### Advisor in thesis

**2020** *Yian Su*. "A Better Memory Understanding for Program Dependence Graph through Static Value-Flow Analysis". Master of Computer Science, Northwestern University, Evanston, US. Committee = Simone Campanoni, Peter Dinda.

**2019** *Michael Leonard*. "PRV Jeeves: A Study of Pseudorandom Value Generator Tradeoffs". Master of Computer Science, Northwestern University, Evanston, US. Committee = Simone Campanoni, Peter Dinda.

### Co-advisor in thesis

**2012** *Pietro Malossi*. "Achieving Platform-Independence for the ILDJIT Compilation Framework". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

**2011** *Andrea Cazzaniga*. "Runtime threads managing in ILDJIT". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Marco Domenico Santambrogio.

**2011** *Diego Mereghetti*. "Definizione di un supporto alla compilazione Just in Time nell'ambito dei sistemi auto adattativi". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Marco Domenico Santambrogio.

**2010** *Luca Rocchini*. "Supporto alla programmazione generica nel compilatore ILDJIT". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

**2009** *Stefano Anelli*. "Method specialization for Common Intermediate Language in a dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

**2009** *Ettore Speziale*. "Multithreading support in ILDJIT dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

**2009** *Michele Tartara*. "ARM code generation and optimization in a dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

**2009** *Marcello Boiardi*. "Scelta automatica di algoritmi di ottimizzazione di codice all'interno del compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Cremona, Italy. Advisor: Prof. Pierluigi San Pietro.

**2009** *Massimiliano Grandi*. "Supporto delle caratteristiche di introspezione dello standard ECMA-335 nel compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Cremona, Italy. Advisor: Prof. Pierluigi San Pietro.

**2008** *Massimiliano Manni, Roberto Molteni*. "Progetto ed implementazione di librerie interne per il supporto dello standard ECMA-335 nel compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

**2008** *Alessandro Assinnata*. "Pianificazione di WSN". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. William Fornaciari.

## Working Experience

**August 2015 – Current** Assistant professor at Northwestern University.

**November 2012 – July 2015** Research Associate at Harvard University.

**November 2009 – October 2012** Postdoctoral Position at Harvard University under both Prof. David Brooks and Prof. Gu-yeon Wei.

**July 2001 – April 2002** Civil service at Gulliver in Cantello (Varese).

**Febr. 2001 – July 2001** Industry worker at Suprema Oggiona S.Stefano building cash registers.

**July 2000 – January 2001** Construction worker for hardwood floors.

**October 1999 – June 2000** Pizza delivery driver

**June 1999 – September 1999** Industrial Electrician

**June 1998 – September 1998** Industrial Electrician

**June 1997 – September 1997** Industrial Electrician

**June 1996 – September 1996** Worked in a greenhouse

## Software and Tools

**2015 – Now** Developed ten LLVM passes that together implement an inter-procedural, alias analysis enhanced constant propagation for a domain-specific language. This software is used in the EECS 323 Code Analysis and Transformation class **CAT**

**Website** www.eecs.northwestern.edu/ simonec/CAT.html

Source Lines of Code: ∼ 1K of C++ 14, ∼ 1k of bash.

**2015 – Now** Developed eight compilers from scratch that together create a compilation pipeline able to translate a subset of the C language down to Intel x86_64 binaries. This software is used in the EECS 322 Compiler Construction class **CC**

**Website** www.eecs.northwestern.edu/ simonec/CC.html

Source Lines of Code: ∼ 40K of C++ 14, ∼ 1k of C, ∼ 3k of bash.

**2015 – Now** Together with Enrico A. Deiana, we developed the **STATS** compiler

Source Lines of Code: ∼ 13K of C++ 14, ∼ 2K of bash script, ∼ 2K of python 2.7

**2015 – Now** Developed the VIRGIL library, which is designed to be used by LLVM passes that generate parallel binaries. This library includes a customizable threadpool, a set of highly-optimized synchronization primitives and data structures. This library is currently used by the STATS compiler.

Source Lines of Code: ∼ 4K of C++ 14

**2017 – 2019** Developed a new backend for ARM in LLVM as well as three middle-end passes to build the **Time Squeezer** compiler

Source Lines of Code: ∼ 4K of C++ 14.

**2010 – 2015** Developed a GPL licensed parallelizing compiler called **HELIX**

**Website** http://helix.eecs.harvard.edu

Source Lines of Code: ∼ 80K of C, ∼ 25k of C++, ∼ 15k of bash.

**2005 – 2014** Developed a GPL licensed compilation framework called **ILDJIT** for the Common Language Infrastructure (CLI) described in the ECMA-335 standard.

**Website** http://ildjit.sourceforge.net

Source Lines of Code: ∼500k of C, ∼ 50k of C++, ∼ 10k of Python, ∼ 35k of bash, ∼ 7k of bison + flex, ∼ 3k of Ruby, ∼ 2k of Java.

**2006 – 2008** Developed a GPL licensed framework to deploy automatically wireless sensors networks (**Swordfish**).

**2005 – 2006** Extended the tuple-based middleware "TinyLime" to exploit sensors. The software has been used in the article "Pervasive games in a mote-enabled virtual world using tuple space middleware". Luca Mottola, Amy Murphy and Gian Pietro Picco. NetGames'06.

**2005 – 2006** Developed a GPL licensed framework for developing agents based on the WSS project.

**2004 – 2005** Developed a GPL licensed world simulator (WSS) for a GNU/Linux system to support the planning of sensor networks using a logic language as input.

**2004** Developed a GPL licensed ontology packet manager for the GNU/Linux systems.

# International scientific collaboration

## Visiting experiences

**January 2014** A week visit at University of Cambridge to collaborate with Dr. Timothy M. Jones and Prof. Robert Mullins in the context of the HELIX project.

**August 2008 – November 2008** Three months visit at Harvard University. I have been involved in the ALARM research project, which is about the hardware process variation problem, under the supervision of Prof. Gu-Yeon Wei and Prof. David Brooks. I designed and implemented the code scheduler algorithm to dynamically reduce the fluctuation of the internal voltage of CPUs.

## Participation in research projects

**2007 – 2009** I have been involved in the OMP European research project at Politecnico di Milano. I was responsible to design and implement a dynamic compiler for the CIL bytecode language for ARM-based embedded platforms.

## Institutions of past and current collaborators

- Northwestern University
- University of Cambridge
- Princeton University
- Harvard University
- Politecnico di Milano
- ST Microelectronics
- INRIA

## Education

**January 2007 — March 2010** Ph.D. studies in Information Technologies at Politecnico di Milano. My dissertation discusses theoretical and practical performance implications of thread level parallelism. To this end, I designed and built a bytecode virtual machine optimized for commodity multicore platforms. I am the author of ILDJIT, a parallel compilation framework that includes static and dynamic compilers as well as a bytecode virtual machine. ILDJIT has been used in several academic and industrial research projects, including the project HELIX that I started during my post-doc.

The Ph.D. was concluded with the highest honors. The advisor was Professor Stefano Crespi Reghizzi.

**Sept. 2004 — July 2006** Engineering studies at Politecnico di Milano. I have been awarded the Master of Science (Laurea specialistica) degree in Computer Engineering (Ingegneria Informatica) with the highest honors (110 Lode). Details on the programs can be found at http://www.deib.polimi.it

During the studies, I developed a tuple based middle-ware extension for the TinyLime based on Lime and TinyOS that allows tuples to be sent on sensors.

In 2005-2006 I have worked on my thesis on an innovative project, building a new distributed virtual machine for the CLI architecture described in the ECMA 335 standard (DotNET). The thesis advisors were Prof. Stefano Crespi Reghizzi and Ing. Giovanni Agosta.

**Sept. 2001 — July 2004** Engineering studies at Politecnico di Milano. I have been awarded the Bachelor of Science (Laurea triennale) degree in Computer Engineering (Ingegneria Informatica) with 108 out of 110 as final mark.

In 2004 I have worked on my thesis on an innovative project, building an ontology packet manager for the GNU/Linux systems. The thesis advisor was Prof. Marco Colombetti.

**Sept. 1995 — July 2000** High-school education at ITIS of Gallarate "Roberto Franceschi" on Telecomunication and electronics.

### School Participation

**Summer 2007** ACACES: Summer School on Advanced Computer Architecture and Compilation for Embedded Systems

## Miscellaneous

- HiPEAC member
- ACM member
- IEEE member