CURRICULUM VITAE ET STUDIORUM

Simone Campanoni

Northwestern University
Department of Computer Science
Mudd building
2233 Tech Drive, Evanston, IL 60208, USA

Phone: +1 (847) 467-3250
Email: simone.campanoni@northwestern.edu
Homepage: http://users.cs.northwestern.edu/∼simonec

Personal Information

Birthdate: April 30th, 1981
Birthplace: Tradate, Italy
Italian and American nationality
Native language: Italian
Foreign language: English
Pronouns: he/him

Current Positions

- Associate professor at the Computer Science department of Northwestern University.
- Courtesy appointment at the Electrical and Computer Engineering department of Northwestern University.

Biography

Simone Campanoni is an associate professor at the Computer Science department of Northwestern University where he runs the ARCANA research lab. Simone's main research area is compilers, with special interest in its relation with computer architecture, runtime systems, operating systems, and programming languages. In more detail, Simone and his research group are passionate about understanding how abstractions used within and around compilers should evolve to better support hardware and applications trends. Hardware constantly evolves to smooth out challenges coming from the materials used. For example, the slowdown of CMOS technology scaling and the increase in power consumption forced hardware to first evolve to multicore chips and then to heterogeneous multi-cores. Abstractions at the compiler boundaries with programming languages, operating systems, and computer architecture need to evolve to properly support these new platforms. Moreover, abstractions used within compilers also need to evolve to better optimize applications that need to run on such platforms. This goal often leads Simone's group to co-design compilers with the computer architecture and operating system they target as well as with the programming language they translate.

List of Sections

Research Interests

Memory-Centric Compilers

Compilers for general-purpose programming languages (e.g., C/C++) have treated computation as the primary driver of performance improvements in programs, leaving memory optimizations as a secondary consideration. Our goal is to enable the next-generation compilers to optimize program's memory like today's compilers do for computation.

Parallelizing Sequential Code

The multicore revolution in microprocessor architecture has left most programs behind. A program that maps easily to multicore architectures is the exception, not the rule. I am interested in showing multiple ways to parallelize the others (e.g., common, sequentially-designed programs) for modern and next-generation architectures.

Compilers for Sub-Cycle Microarchitecture Activities

Safety margins in conventional architectures are conservative to *always* avoid computational errors leading to energy inefficiencies. Resilient architectures squeeze these margins to save energy, correcting errors through costly rollback. Co-designed compilers can help resilient architectures to reduce their overhead by adapting the running code to their run-time characteristics.

The power of modern compilers for the hardware-software stack

Modern compilers are more powerful than what they are currently used for. This research direction shows how modern compilers create opportunities to reconsider the abstractions used between the layers of the hardware-software stack. Changing such abstractions generates important benefits compared to how we have been designing systems.

Prior research

Mining Advantages in Randomized Code (MARC)

The application landscape is rapidly evolving, including more often randomized algorithms. Current compilers ignore whether or not a program being compiled is randomized, leaving important opportunities unexplored. The MARC research project aims to identify and exploit such opportunities.

Bytecode Virtual Machines Virtual machines designed to execute bytecode programs are everywhere. The most successful and widely-adopted examples are Java and .NET. Browsers are virtual machines as well thanks to their ability to run programs written in multiple languages (e.g., JavaScript).
A bytecode virtual machine usually includes several components. Code generators, code optimizers, garbage collectors, execution engine, and profilers are the most common ones. Understanding interactions of these components allows them to be co-designed, which open interesting optimization opportunities. To enable these studies, we built the open source ILDJIT compilation framework.
An example of these optimizations is the dynamic look-ahead (DLA). In DLA, code generators and optimizers are driven by feedback coming from the execution engine to suppress dynamic compilation latency.

Awards

Research

"*Automatically Accelerating Non-Numerical Programs By Extracting Threads with an Architecture-Compiler Co-Design*"

Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks
Communication ACM Research Highlights, December 2017

Research Highlights 2017

"*Automatically Accelerating Non-Numerical Programs By Architecture-Compiler Co-Design*"
Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks
IEEE Micro's Top Picks Honorable Mention in Computer Architecture Conferences

Top Picks Honorable mentions 2015

"*HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs*"

Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks
HiPEAC award for the ISCA 2014 paper

award 2014

"*The HELIX Project: Overview and Directions*"

Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks
HiPEAC award for the DAC 2012 paper

award 2012

"*Metronome: Operating System Level Performance Management via Self-Adaptive Computing*"

Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto and Marco D. Santambrogio
HiPEAC award for the DAC 2012 paper

award 2012

"*Voltage Noise in Production Processors*"

Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks
IEEE Micro's Top Picks in Computer Architecture Conferences

Top Picks 2011

"*Dynamic Compilation and Parallelism: Theory and large scale experimentation*"

Simone Campanoni
Ph.D. with the highest honors. Politecnico di Milano, 3 March 2010.

Highest honors
2010

"*A parallel dynamic compiler for CIL bytecode*"

Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi
Best paper for the PhDay at Politecnico di Milano, 2008

Best paper
2008

Teaching

"*Best Teacher Award of the EECS Department*"

Northwestern University

Best teacher
2018

Publications

For clustering publications following different criterias (by year, by project, by area, or by venue), please go here. Next are the publications in chronological order starting from the conference ones. Icons are clickable.

International Conferences

"*Saving Energy with Per-Variable Bitwidth Speculation*" **ASPLOS**
Tommy McMichen, David Dlott, Panitan Wongse-ammat, Nathan Greiner, Hussain Khajanchi, Russ Joseph, and Simone Campanoni 2025
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems

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"*Representing Data Collections in an SSA Form*" **CGO**
Tommy McMichen, Nathan Greiner, Peter Zhong, Federico Sossai, Atmn Patel, and Simone Campanoni 2024
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 32.5% (37/114)

Awarded badges from the Artifact Evaluation Committee:
Available: Reusable: Reproduced:

"*Compiling Loop-Based Nested Parallelism for Irregular Workloads*" **ASPLOS**
Yian Su, Mike Rainey, Nicholas Wanninger, Nadharm Dhiantravan, Jasper Liang, Umut A. Acar, Peter Dinda, and Simone Campanoni 2024
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems

Awarded badges from the Artifact Evaluation Committee:
Available: Functional: Reproduced:

"*Getting a Handle on Unmanaged Memory*" **ASPLOS**
Nicholas Wanninger, Tommy McMichen, Simone Campanoni, and Peter Dinda 2024
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems

Awarded badges from the Artifact Evaluation Committee:
Available: Functional: Reproduced:

"*TrackFM: Far-out Compiler Support for a Far Memory World*" **ASPLOS** 2024
Brian R. Tauro, Brian Suchy, Simone Campanoni, Peter Dinda, and Kyle C. Hale
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems

 BibTeX  GitHub

Awarded badges from the Artifact Evaluation Committee:

Available:  Functional:  Reproduced: 

"*PROMPT: A Fast and Extensible Memory Profiling Framework*" **OOPSLA** 2024
Ziyang Xu, Yebin Chon, Yian Su, Zujun Tan, Sotiris Apostolakis, Simone Campanoni, and David I. August
In proceedings of the International Conference on Object-Oriented Programming, Systems, Languages, and Applications
Acceptance rate: 30.9% (38/123)

 BibTeX  GitHub

Awarded badges from the Artifact Evaluation Committee:

Available:  Reusable: 

"*CAMP: Compiler and Allocator-based Heap Memory Protection*" **USENIX Security** 2024
Zhenpeng Lin, Zheng Yu, Ziyi Guo, Simone Campanoni, Peter Dinda, and Xinyu Xing
In proceedings of the USENIX Security Symposium

 BibTeX   GitHub

Awarded badges from the Artifact Evaluation Committee:

Available:  Functional:  Reproduced: 

"*GhOST: a GPU Out-of-Order Scheduling Technique for stall reduction*" **ISCA** 2024
Ishita Chaturvedi, Bhargav Reddy Godala, Yucan Wu, Ziyang Xu, Konstantinos Iliakis, Panagiotis-Eleftherios Eleftherakis, Sotirios Xydis, Dimitrios Soudris, Tyler Sorensen, Simone Campanoni, Tor M. Aamodt, and David I. August
In proceedings of the International Symposium on Computer Architecture
Acceptance rate: 21.2% (79/372)

 BibTeX 

Awarded badges from the Artifact Evaluation Committee:

Available:  Functional:  Reproduced: 

"*Revisiting Computation for Research: Practices and Trends*" **SC**
Jeremiah Giordani, Ziyang Xu, Ella Colby, August Ning, Bhargav Reddy Godala, Ishita Chaturvedi, Shaowei Zhu, Yebin Chon, Greg Chan, Zujun Tan, Galen Collier, Jonathan D. Halverson, Enrico Armenio Deiana, Jasper Liang, Federico Sossai, Yian Su, Atmn Patel, Bangyen Pham, Nathan Greiner, Simone Campanoni, and David I. August 2024
In proceedings of the High Performance Computing, Networking, Storage and Analysis
Acceptance rate: 22.7% (102/449)

 BibTeX  IEEE

Awarded badges from the Artifact Evaluation Committee:

Available: 

"*Guess and Sketch: Language Model Guided Transpilation*" **ICLR**
Celine Lee, Abdulrahman Mahmoud, Michal Kurek, Simone Campanoni, David M. Brooks, Stephen Chong, Gu-Yeon Wei, and Alexander M. Rush 2024
In proceedings of the International Conference on Learning Representations

 BibTeX

"*EMISSARY: Enhanced Miss Awareness Replacement Policy for L2 Instruction Caching*" **ISCA**
Nayana Prasad Nagendra, Bhargav Reddy Godala, Ishita Chaturvedi, Atmn Patel, Svilen Kanev, Tipp Moseley, Jared Stark, Gilles A. Pokam, Simone Campanoni, and David I. August 2023
In proceedings of the International Symposium on Computer Architecture
Acceptance rate: 21.2% (79/372)

 BibTeX  

"*SPLENDID: Supporting Parallel LLVM-IR Enhanced Natural Decompilation for Interactive Development*" **ASPLOS**
Zujun Tan, Yebin Chon, Michael Kruse, Johannes Doerfert, Ziyang Xu, Brian Homerding, Simone Campanoni, and David I. August 2023
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems
Acceptance rate: 26.7% (72/270)

 BibTeX  

Awarded badges from the Artifact Evaluation Committee:

Available:  Functional:  Reproduced: 

"*Program State Element Characterization*" **CGO**
Enrico Armenio Deiana, Brian Suchy, Michael Wilkins, Brian Homerding, Tommy McMichen, Katarzyna Dunajewski, Peter Dinda, Nikos Hardavellas, and Simone Campanoni 2023
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 39.2% (20/51)

 BibTeX  

Awarded badges from the Artifact Evaluation Committee:

Available:  Functional:  Reproduced: 

"*WARDen: Specializing Cache Coherence for High-Level Parallel Languages*" **CGO**
Michael Wilkins, Sam Westrick, Vijay Kandiah, Alex Bernat, Brian Suchy, Enrico Armenio Deiana, Simone Campanoni, Umut A. Acar, Peter Dinda, and Nikos Hardavellas 2023
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 39.2% (20/51)

 BibTeX 

Awarded badges from the Artifact Evaluation Committee:

Available:  Reusable: 

"*WARio: Efficient Code Generation for Intermittent Computing*" **PLDI**
Vito Kortbeek, Souradip Ghosh, Josiah Hester, Simone Campanoni, and Przemysław Pawełczak 2022
In proceedings of the International Conference on Programming Language Design and Implementation
Acceptance rate: 20.9% (68/326)

   

Awarded badges from the Artifact Evaluation Committee:

Available:  Reusable: 

"*CARAT CAKE: Replacing Paging via Compiler/Kernel Cooperation*" **ASPLOS**
Brian Suchy, Souradip Ghosh, Aaron Nelson, Zhen Huang, Drew Kersnar, Siyuan Chai, Michael Cuevas, Alex Bernat, Gaurav Chaudhary, Nikos Hardavellas, Simone Campanoni, and Peter Dinda 2022
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems
Acceptance rate: 20.2% (80/397)

 BibTeX  

Awarded badges from the Artifact Evaluation Committee:

Available: 

"*NOELLE Offers Empowering LLVM Extensions*" **CGO**
Angelo Matni, Enrico Armenio Deiana, Yian Su, Lukas Gross, Souradip Ghosh, Sotiris Apostolakis, Ziyang Xu, Zujun Tan, Ishita Chaturvedi, Brian Homerding, Tommy McMichen, David I. August, and Simone Campanoni 2022
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 28.7% (27/94)

 BibTeX    

Awarded badges from the Artifact Evaluation Committee:

Available:  Functional:  Reproduced: 

"*Quantifying the Semantic Gap Between Serial and Parallel Programming*" **IISWC**
Xiaochun Zhang, Timothy M. Jones, and Simone Campanoni 2021
In proceedings of the International Symposium on Workload Characterization
Acceptance rate: 39.6% (19/48)

 BibTeX  

"*Paths to OpenMP in the Kernel*" **SC**
Jiacheng Ma, Wenyi Wang, Aaron Nelson, Michael Cuevas, Brian Homerding, Conghao Liu, Zhen Huang, Simone Campanoni, Kyle C. Hale, and Peter Dinda 2021
In proceedings of the High Performance Computing, Networking, Storage and Analysis
Acceptance rate: 26.8% (98/365)

 BibTeX  

"*Task Parallel Assembly Language for Uncompromising Parallelism*" **PLDI**
Mike Rainey, Kyle C. Hale, Ryan Newton, Nikos Hardavellas, Simone Campanoni, Peter Dinda, and Umut A. Acar 2021
In proceedings of the International Conference on Programming Language Design and Implementation
Acceptance rate: 27.2% (87/320)

 BibTeX 

Awarded badges from the Artifact Evaluation Committee:

Functional: 

"*CODE: Compiler-Based Neuron-Aware Ensemble Training*" **MLSys**
Ettore M. G. Trainiti, Thanapon Noraset, David Demeter, Doug Downey, and Simone Campanoni 2021
In proceedings of the Machine Learning and Systems
Acceptance rate: 24.1% (52/216)

 BibTeX

"*Compiler-based Timing For Extremely Fine-grain Preemptive Parallelism*" **SC**
Souradip Ghosh, Michael Cuevas, Simone Campanoni, and Peter Dinda 2020
In proceedings of the High Performance Computing, Networking, Storage and Analysis
Acceptance rate: 25.1% (95/378)

 BibTeX  

"*SCAF: A Speculation-Aware Collaborative Dependence Analysis Framework*" **PLDI**
Sotiris Apostolakis, Ziyang Xu, Zujun Tan, Greg Chan, Simone Campanoni, and David I. August 2020
In proceedings of the International Conference on Programming Language Design and Implementation
Acceptance rate: 22.6% (77/341)

 BibTeX   
Awarded badges from the Artifact Evaluation Committee:
Available:  Reusable:  Functional: 

"*CARAT: A Case for Virtual Memory through Compiler- And Runtime-based Address Translation*" **PLDI**
Brian Suchy, Simone Campanoni, Nikos Hardavellas, and Peter Dinda 2020
In proceedings of the International Conference on Programming Language Design and Implementation
Acceptance rate: 22.6% (77/341)

 BibTeX 

"*Perspective: A Sensible Approach to Speculative Automatic Parallelization*" **ASPLOS**
Sotiris Apostolakis, Ziyang Xu, Greg Chan, Simone Campanoni, and David I. August 2020
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems
Acceptance rate: 18.1% (86/476)

 BibTeX   
Awarded badges from the Artifact Evaluation Committee:
Available:  Reusable: 

"*Introducing the Pseudorandom Value Generator Selection in the Compilation Toolchain*" **CGO**
Michael Leonard, and Simone Campanoni 2020
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 27.4% (26/95)

 BibTeX 

"*Time Squeezing for Tiny Devices*" **ISCA**
Yuanbo Fan, Simone Campanoni, and Russ Joseph 2019
In proceedings of the International Symposium on Computer Architecture
Acceptance rate: 17.0% (62/365)

 BibTeX   

"*Workload Characterization of Nondeterministic Programs Parallelized by STATS*" **ISPASS**
Enrico Armenio Deiana, and Simone Campanoni 2019
In proceedings of the International Symposium on Performance Analysis of Systems and Software
Acceptance rate: 29.5% (26/88)

 BibTeX 

"*Compiler-guided instruction-level clock scheduling for timing speculative processors*" **DAC**
Yuanbo Fan, Tianyu Jia, Jie Gu, Simone Campanoni, and Russ Joseph 2018
In proceedings of the Design Automation Conference
Acceptance rate: 24.3% (168/691)

 BibTeX 

"*Unconventional Parallelization of Nondeterministic Applications*" **ASPLOS**
Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, and Simone Campanoni 2018
In proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems
Acceptance rate: 17.6% (56/319)

 BibTeX 

"*Performance Implications of Transient Loop-Carried Data Dependences in Automatically Parallelized Loops*" **CC**
Niall Murphy, Timothy M. Jones, Robert Mullins, and Simone Campanoni 2016
In proceedings of the International Conference on Compiler Construction
Acceptance rate: 31.2% (24/77)

 BibTeX 

"*HELIX-UP: Relaxing Program Semantics to Unleash Parallelization*" **CGO**
Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David M. Brooks 2015
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 27.3% (24/88)

 BibTeX  

One of four papers nominated for the Best Paper Award by the Program Committee

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"*Power-Awareness and Smart-Resource Management in Embedded Computing Systems*" **CODES+ISSS**
Alessandro A. Nacci, Gianluca C. Durelli, Josue Pagan, Marina Zapater, Matteo Ferroni, Riccardo Cattaneo, Monica Vallejo, Simone Campanoni, Jose Ayala, and Marco D. Santambrogio 2015
In proceedings of the International Conference on Hardware/Software Codesign and System Synthesis
Invited paper

 BibTeX  IEEE

"*HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs*" **ISCA**
Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei, and David M. Brooks 2014
In proceedings of the International Symposium on Computer Architecture
Acceptance rate: 17.8% (46/258)

 BibTeX  IEEE

IEEE Micro's Top Picks in Computer Architecture Conferences honorable mention, 2014
Communication ACM Research Highlights (CACM), 2017

"*HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing*" **CGO**
Simone Campanoni, Timothy M. Jones, Glenn Holloway, Vijay Janapa Reddi, Gu-Yeon Wei, and David M. Brooks 2012
In proceedings of the International Symposium on Code Generation and Optimization
Acceptance rate: 28.9% (26/90)

 BibTeX 

"*The HELIX Project: Overview and Directions*" **DAC**
Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei, and David M. Brooks 2012
In proceedings of the Design Automation Conference
Invited paper

 BibTeX  IEEE

"*Metronome: Operating System Level Performance Management via Self-Adaptive Computing*" **DAC**
Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto, and Marco D. Santambrogio 2012
In proceedings of the Design Automation Conference
Acceptance rate: 22.7% (168/741)

 BibTeX  IEEE

"*Voltage Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software-guided Thread Scheduling*" **MICRO**
Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei, and David M. Brooks 2010
In proceedings of the International Symposium on Microarchitecture
Acceptance rate: 18.1% (45/248)

 BibTeX  IEEE

IEEE Micro's Top Picks in Computer Architecture Conferences, 2011

"*Software-Assisted Hardware Reliability: Abstracting Circuit-level Challenges to the Software Stack*" **DAC**
Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Michael D. Smith, Gu-Yeon Wei, and David M. Brooks 2009
In proceedings of the Design Automation Conference
Acceptance rate: 21.7% (148/682)

 BibTeX  IEEE

"*Dynamic Look Ahead Compilation: a technique to hide JIT compilation latencies in multicore environment*" **CC**
Simone Campanoni, Martino Sykora, Giovanni Agosta, and Stefano Crespi Reghizzi 2009
In proceedings of the International Conference on Compiler Construction
Acceptance rate: 25.0% (18/72)

 BibTeX  GitHub

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"*Traces of Control-Flow Graphs*" **DLT**
Simone Campanoni, and Stefano Crespi Reghizzi 2009
In proceedings of the International Conference on Developments in Language Theory
Acceptance rate: 45.7% (32/70)

 BibTeX

"*Multi-level Design and Optimization of Wireless Sensor Networks*" **INSS**
Simone Campanoni, and William Fornaciari 2008
In proceedings of the International Conference on Networked Sensing Systems

 BibTeX IEEE

"*Node-Level Optimization of Wireless Sensor Networks*" **WiCom**
Simone Campanoni, and William Fornaciari 2008
In proceedings of the International Conference on Wireless Communications, Networking and Mobile Computing

 BibTeX IEEE

"*Models and Tradeoffs in WSN System-Level Design*" **DSD**
Simone Campanoni, and William Fornaciari 2008
In proceedings of the Euromicro Symposium on Digital System Design

 BibTeX IEEE

"*Ensuring Feasibility of Wireless Sensor Networks*" **ICCSC**
Simone Campanoni, and William Fornaciari 2008
In proceedings of the International Conference on Circuits and Systems for Communications

 BibTeX IEEE

"*SWORDFISH: A framework to formally design WSNs capturing events*" **SoftCOM**
Simone Campanoni, and William Fornaciari 2007
In proceedings of the International Conference on Software, Telecommunications and Computer Networks

 BibTeX IEEE

Magazines

- Georgios Tziantzioulis, Nikos Hardavellas and Simone Campanoni. "Temporal Approximate Function Memoization". **IEEE Micro** special issue on approximate computing, 9 August 2018. IEEE computer Society Digital Library. IEEE Computer Society.
- Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks. "Automatically Accelerating Non-Numerical Programs By Extracting Threads with an Architecture-Compiler Co-Design". Communication ACM Research Highlights (**CACM**), December 2017.
- Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks. "HELIX: Making the Extraction of Thread-Level Parallelism Mainstream". **IEEE Micro**, 12 June 2012. IEEE computer Society Digital Library. IEEE Computer Society.
- Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise in Production Processors". **IEEE Micro**'s Top Picks in Computer Architecture Conferences. Vol. 3, no. 1, 2011.

International Journals

- Ling Jin, Yinzhi Cao, Yan Chen, Di Zhang, Simone Campanoni. "EXGEN: Cross-platform, Automated Exploit Generation for Smart Contract Vulnerabilities". IEEE Transactions on Dependable and Secure Computing. 2023.
- Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Kim Hazelwood, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Eliminating Voltage Emergencies via Software-Guided Code Transformations". ACM Transactions on Architecture and Code Optimization (**TACO**). Vol. 7, no. 2, 2010.
- Simone Campanoni, Giovanni Agosta, Stefano Crespi Reghizzi and Andrea Di Biagio. "A highly flexible, parallel virtual machine: design and experience of ILDJIT". Software: Practice and Experience (**SPE**). Vol. 40, no. 2, 2010.

Books

- Simone Campanoni. "Guide to ILDJIT". Springer. 1st Edition. September 2011. ISBN: 978-1-4471-2193-0.

Book Chapters

- Marcello Mura, Simone Campanoni, William Fornaciari, Mariagiovanna Sami. "Optimal Design of Wireless Sensor Networks". Chapter 19 of "Methodologies and Technologies for Networked Enterprises", in Lecture Notes in Computer Science, Vol. 7200, Anastasi, G.; Bellini, E.; Di Nitto, E.; Ghezzi, C.; Tanca, L.; Zimeo, E. (Eds.), 2012, ISBN 978-3-642-31738-5, July 2012.

Short Papers

- Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, Simone Campanoni. "The Liberation Day of Nondeterministic Programs". 26th International Conference on Parallel Architectures and Compilation Techniques (**PACT**). Portland, Oregon, USA, September 9-13, 2017.
- Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "ILDJIT: a parallel dynamic compiler". In proceedings of 16th IFIP/IEEE International Conference on Very Large Scale Integration (**VLSI-SoC**), Rhodes Island, Greece, October 13-15, 2008.

International Workshops

- Bhargav Reddy Godala, Ishita Chaturvedi, Yucan Wu, Simone Campanoni, and David I. August. "QPoints: QEMU to gem5 ARM Full System Checkpointing". The gem5 Workshop, June 2023.
- Bhargav Reddy Godala, Nayana Prasad Nagendra, Ishita Chaturvedi, Simone Campanoni, and David I. August. "Modern Front-end Support in gem5". The gem5 Workshop, June 2023.
- Kyle C. Hale, Simone Campanoni, Nikos Hardavellas, and Peter Dinda. "The Case for an Interwoven Parallel Hardware/Software Stack". International Workshop on Runtime and Operating Systems for Supercomputers (**ROSS**). St. Louis, Missouri, USA. November 15, 2021.
- Khalid Al-Hawaj, Simone Campanoni, Gu-Yeon Wei, David Brooks. "Unified Cache: A Case for Low-Latency Communication". 3rd International Workshop on Parallelism in Mobile Platforms (**PRISM**). Portland, OR, USA. June 13-17, 2015.
- Niall Murphy, Timothy M. Jones, Simone Campanoni, Robert Mullins. "Limits of Static Dependence Analysis for Automatic Parallelization". 18th International Workshop on Compilers for Parallel Computing (**CPC**). London, UK. January 7-9, 2015.
- Simone Campanoni, Svilen Kanev, Kevin Brownell, Gu-Yeon Wei and David Brooks. "Breaking Cyclic-Multithreading Parallelization with XML Parsing". 2nd International Workshop on Parallelism in Mobile Platforms (**PRISM**). Minneapolis, Minnesota, USA, June 14, 2014.
- Simone Campanoni and Luca Rocchini. "Static Memory Management within Bytecode Languages on Multicore Systems". In proceedings of Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (**CHANGE**). Newport Beach, California, March 6, 2011.
- Michele Tartara, Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "Parallelism and Retargetability in the ILDJIT Dynamic Compiler". 23th International Conference on Architecture of Computing Systems (**ARCS**). Hannover, Germany, February 22th, 2010.

- Michele Tartara, Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "Just-In-Time compilation on ARM processors". In proceedings of ACM 4th Workshop on the Implementation, Compilation, Optimization of Object-Oriented Languages, Programs and Systems (**ICOOOLPS**). Genova, Italy, July 6th, 2009.
- Vijay Janapa Reddi, Meeta S. Gupta, Krishna K. Rangan, Simone Campanoni, Glenn Holloway, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise: Why It's Bad, and What To Do About It". In proceedings of IEEE 2009 5th Workshop on Silicon Errors in Logic - System Effects (**SELSE**), Stanford University, March 24th and 25th, 2009.
- Stefano Crespi Reghizzi and Simone Campanoni. "Traces of control-flow graphs". ESF Workshop on Developments and New Tracks in Trace Theory, Cremona, Italy, 9-11 October 2008.

Italian National Conferences

- Simone Campanoni, Michele Tartara, and Stefano Crespi Reghizzi. "ILDJIT: A parallel, free software and highly flexible Dynamic Compiler". IV Conferenza Italiana sul Software Libero. Cagliari, Italy, 11 - 12 June 2010.
- Michele Tartara, Stefano Crespi Reghizzi and Simone Campanoni. "Extending hammocks for parallelism detection". Italian Conference on Theoretical Computer Science (ICTCS). Camerino, Italy, 15 - 17 September 2010.
- Simone Campanoni. "Parallelism on compilation and execution". PhDay at Politecnico di Milano, Milan, Italy, June 24, 2009.
- Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". PhDay at Politecnico di Milano, Best paper, Milan, Italy, June 26, 2008.

Posters

- Mike Rainey, Simone Campanoni, Peter Dinda, Umut Acar, Yian Su, Nick Wanninger, Jasper Liang, and Nadharm Dhiantravan. "Automatic granularity control for fork-join parallelism on multicore systems". The 10th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2023.
- Brian Richard Tauro, Brian Suchy, Simone Campanoni, Peter Dinda, Kyle C. Hale. "TrackFM: Far-out Compiler Support for a Far Memory World". The 10th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2023.
- Simone Campanoni, Yan Chen, Hai Zhou. "RINGS: Accelerating the NextG Protocols Definition to Code Generation with an Automatic and Secure Verification-Compilation Tool-Chain". NSF. October 2022.
- Simone Campanoni. "The MARC compiler: Mining Advantages in non-deteRministic Code". ARM Summit. September 2019.
- Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, and Simone Campanoni. "Unconventional Parallelization of Nondeterministic Applications". The 7th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2018.
- Georgios Tziantzioulis, Nikos Hardavellas and Simone Campanoni. "Temporal Approximate Function Memoization". The 6th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2017.
- Enrico Armenio Deiana, Vincent St-Amour, Peter Dinda, Nikos Hardavellas, Simone Campanoni. "Soft Dependences: Who They Are, Where to Find Them, and How to Satisfy Them". The 6th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2017.

- Georgios Tziantzioulis, Haiyang Han, Nikos Hardavellas, Simone Campanoni. "Temporal Output Memoization". The 5th Greater Chicago Area Systems Research Workshop (**GCASR**). April 2016.
- Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks. "Relaxing Program Semantics to Unleash Parallelization". In the Center for Future Architectures Research (C-FAR). November 2014.
- Michael Lyons, Judson Porter, Yakun Sophia Shao, Simone Campanoni, David Brooks. "Architecture Design for Fine-grained Hardware Acceleration". In The Gigascale Systems Research Center(GSRC) Annual Symposium, September 2010.
- Simone Campanoni. "Dynamic Compilation and Parallelism. Theory and Large Scale Experimentation". PhDay at Politecnico di Milano, Milan, Italy, June 26, 2009.
- Simone Campanoni. "ILDJIT: Intermediate Language Distributed Just In Time". PhDay at Politecnico di Milano, Milan, Italy, June 24, 2009.

Theses

1. Simone Campanoni. "Dynamic Compilation and Parallelism: Theory and large scale experimentation". PhD Dissertation, December 2009.

2. Simone Campanoni. "Intermediate Language Distributed Just In Time for the CIL Bytecode". Master Thesis, July 2006.

3. Simone Campanoni. "Ontology Packet Manager". Bachelor Thesis, July 2004.

Technical Reports

4. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". SIGPLAN Notices, Volume 43, Number 4, April, 2008.

5. Simone Campanoni and William Fornaciari. "Design and optimization of Wireless Sensor Networks". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 17, Anno 2008.

6. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 3, Anno 2008.

7. Simone Campanoni and William Fornaciari. "Board-Level clustering of sensor network nodes". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 61, Anno 2007.

Tutorials

1. "Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with the 12th ISPA Conference). Milan, Italy. August 29th, 2014. Full day tutorial.

2. "ILDJIT: Hands-On ILDJIT for Static and Dynamic Program Analysis and Transformation". Presented at International Symposium on Code Generation and Optimization (CGO), April 2012. Full day tutorial.

3. "ILDJIT: a Compilation Framework for Static and Dynamic Program Analysis and Optimization". Presented at the 44th International Symposium on Microarchitecture (MICRO), December, 2011. Full day tutorial.

4. "ILDJIT: a compilation framework for program introspection, optimization and micro-architectural design." Presented at High-Performance and Embedded Architectures and Compilers (HiPEAC), January 2011. Half day tutorial.

5. "ILDJIT Compiler Framework for Architecture Research". Presented at the 43rd International Symposium on Microarchitecture (MICRO), December 4th, 2010. Half day tutorial.

US Patents

1. "Compiler-based neuron-aware deep neural network ensemble training". Ettore Maria Giuseppe Trainiti, Simone Campanoni, Doug Downey. US 2022/0284297. Submitted 2022.

2. "Methods and apparatus for parallel processing". Simone Campanoni, Gu-Yeon Wei, David Brooks, Kevin Brownell, Svilen Kanev. US20160313991A1. Submitted: 2013. Granted: 2021.

Funding

Total:

- $2,892,227 for personal share
- $5,752,127 for Northwestern University
- $10,973,755 across institutions

We are grateful that we received funding from the National Science Foundation (NSF), the Department of Energy (DOE), and companies like ARM. Next are more detail about the funding we received.

National Science Foundation

May 2022 – April 2025 National Science Foundation
Co-PI of "RINGS: Accelerating the NextG Protocols Definition to Code Generation with an Automatic and Secure Verification-Compilation Tool-Chain"
NSF RINGS-2148177
This project is in collaboration with

- (PI) Prof. Yan Chen (Northwestern University)
- Prof. Hai Zhou (Northwestern University)

Amount:

- $300,000 for personal share
- $899,998 for Northwestern University

October 2021 – September 2025 National Science Foundation
Co-PI of "Collaborative Research: PPoSS: LARGE: Unifying Software and Hardware to Achieve Performant and Scalable Frictionless Parallelism in the Heterogeneous Future"
NSF PPoSS-2119069
This project is in collaboration with

- (PI) Prof. Peter Dinda (Northwestern University)
- Prof. Nikos Hardavellas (Northwestern University)
- Prof. Umut Acar (Carnegie Mellon University)
- Prof. Guy Blelloch (Carnegie Mellon University)

Amount:

- $642,484 for personal share
- $1,927,454 for Northwestern University
- $4 Millions across institutions

October 2021 – September 2025 National Science Foundation
PI of "Collaborative Research: SHF: Medium: Collaborative Automatic Parallelization"
NSF CCF-2107042
This project is in collaboration with

- Prof. David I. August (Princeton University)

Amount:

- $600,000 for personal share
- $1.2 Million across institutions

July 2021 – June 2023 National Science Foundation
PI of "Collaborative Research: PPoSS: Planning: A Disciplined Approach to Scaling in the Post-Moore's Law Era"
NSF CCF-2118708
This project is in collaboration with

- Prof. David I. August (Princeton University)

Amount:

- $91,300 for personal share
- $250,000 across institutions

October 2020 – September 2022 National Science Foundation
Co-PI of "Collaborative Research: PPoSS: Planning: Unifying Software and Hardware to Achieve Performant and Scalable Zero-cost Parallelism in the Heterogeneous Future"
NSF PPoSS-2028851
This project is in collaboration with

- (PI) Prof. Peter Dinda (Northwestern University)
- Prof. Nikos Hardavellas (Northwestern University)
- Prof. Kyle Hale (Illinois Institute of Technology)
- Prof. Umut Acar (Carnegie Mellon University)

Amount:

- $42,781 personal share
- $128,343 for Northwestern University
- $250,000 across institutions

REU supplements:

- REU supplement: Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2021, $16,000

October 2019 – September 2023 National Science Foundation
PI of "SHF: Small: The Compiler-Architecture Solution to the Data Dependent, Circuit-Level Critical-Paths Variations"
NSF CCF-1908488
This project is in collaboration with

- Prof. Russell Joseph (Northwestern University)

Amount:

- $249,871 for personal share
- $499,741 for Northwestern University

REU supplements:

- REU supplement: Simone Campanoni (PI), Russell Joseph, 2020, $24,000

September 2018 – August 2023 National Science Foundation
Co-PI of "CSR: Medium: Collaborative Research: Interweaving the Parallel Software/Hardware Stack"
NSF CNS-1763743
This project is in collaboration with

- (PI) Prof. Peter Dinda (Northwestern University)
- Prof. Nikos Hardavellas (Northwestern University)
- Prof. Kyle Hale (Illinois Institute of Technology)

Amount:

- $303,119 for personal share
- $909,275 for Northwestern University
- $1.25 Million across institutions

REU supplements:

- REU supplement: Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2022, $16,000
- REU supplement: Peter A. Dinda (PI), Nikos Hardavellas, Simone Campanoni, 2020, $16,000

Department of Energy

September 2021 – August 2024 Department of Energy X-Stack

Co-PI of "X-CELLENT: X-Compiler Extending LLVM for Enhanced Natural Translation", DOE 0000260915.
This project is in collaboration with

- (PI) Prof. David I. August (Princeton University)
- Dr. Michael Kruse

Amount:

- $600,000 for personal share
- $2.5 Million across institutions

Industry

November 2019 – December 2020 ARM

This funding is related to the paralleilzing compiler research direction.
Amount:

- $40,000 personal share

January 2011 – December 2011 Microsoft Research

This funding was raised with Prof. David Brooks.
Amount: $20,000

December 2010 – March 2011 HiPEAC

This funding is related to ILDJIT.
Amount: €8,000

January 2007 – December 2009 ST Microelectronics

This funding covered the expenses of my PhD studies.

Academia

September 2001 – July 2006 Politecnico di Milano

University scholarship awarded by regional institute (competitive scholarship based on GPA, credit hours earned and financial need).

Academic and Professional Service

Steering Committee

- International Symposium on Microarchitecture (MICRO). 2023.

General Chair

- International Symposium on Microarchitecture (MICRO). 2022. Co-General chair with Nikos Hardavellas.

Program Chair

- Program Co-Chair with Martina Maggio and Antonio Fernández at the 13-th IEEE "International Symposium on Parallel and Distributed Processing with Applications" (ISPA). Helsinki, Finland. August 20-22, 2015.

  Website http://research.comnet.aalto.fi/ISPA2015

- Program Co-Chair with Martina Maggio at the 12-th IEEE "International Symposium on Parallel and Distributed Processing with Applications" (ISPA). Milan, Italy. August 25-29, 2014.

  Website http://ispa14.necst.it

- Program Co-Chair at the 2nd edition of the IEEE Workshop on "Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments", (co-located with DAC), San Francisco, USA, June 3, 2012.

  Website http://change.ws.dei.polimi.it

- Vice-chairs of the track "Embedded Software and Optimization" at the 10th edition of the IEEE/IFIP "International Conference on Embedded and Ubiquitous Computing". Paphos, Cyprus. October 3-5, 2012.

Program Committee

- International Symposium on Computer Architecture (ISCA). 2025.
- International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS). 2025, 2024, 2023.
- International Symposium on Code Generation and Optimization (CGO). 2024, 2022, 2020, 2019, 2017, 2015.
- IEEE Micro Top Picks. 2025.
- International Symposium on Microarchitecture (MICRO). 2024, 2023, 2017.
- International Parallel and Distributed Processing Symposium (IPDPS). 2023.
- International Symposium on Performance Analysis of Systems and Software (ISPASS). 2024, 2023, 2019.
- International Conference on Compiler Construction (CC). 2024, 2021.
- International Conference on Parallel Architectures and Compilation Techniques (PACT). 2020.
- International Symposium on Workload Characterization (IISWC). 2018.
- International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES). 2020.

- International Conference on Parallel Processing (ICPP). 2020.
- International Conference on Computing Frontiers (CF). 2017, 2016.
- International Symposium on Parallel and Distributed Processing with Applications (ISPA). 2016.
- 3rd edition of the workshop Parallelism in Mobile Platforms (PRISM). 2015.
- DAC Workshop on Suite of Embedded Applications and Kernels (SEAK). 2014.
- International Symposium on Embedded Multicore Systems-on-chip (MCSoC). 2013, 2012.
- 11th edition of the IEEE/IFIP International Conference on Embedded and Ubiquitous Computing. 2013.
- 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC). 2013.
- Special session "Self-adaptable and autonomic systems" at the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC). 2012.
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing. 2011.
- 1st edition of the Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE), (co-located with ASPLOS). 2011.
- 1st edition of the Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (2 PARMA), (co-located with ARCS). 2010.

Financial Chair

- International Symposium on Performance Analysis of Systems and Software (ISPASS). 2020.

Special Session Organizer

- Organizer together with Donatella Sciuto. Special session "Power-awareness and resource management in mobile and IoT computing systems".
- Organizer together with Lamia Youseff. Special session "The Future of Operating Systems for Embedded Systems and Software (ESS)" at the 50th Design Automation Conference (DAC), Austin, Texas, USA.
- Session chair of the special session "The Future of Operating Systems for Embedded Systems and Software (ESS)" at the 50th Design Automation Conference (DAC), Austin, Texas, USA.

Journal and Magazine Reviewer

- Reviewer of the ACM Transactions on Architecture and Code Optimization (TACO) 2022, 2021, 2019, 2017, 2015, 2014, 2013, 2012
- Reviewer of the IEEE Transactions on Computers (TC) 2022
- Reviewer of the Microprocessors and Microsystems journal, Elsevier 2017, 2016.
- Reviewer of the IEICE Transactions on Information and Systems 2017.
- Reviewer of the IEEE Computer Architecture Letters 2015.
- Reviewer of the journal Computer 2015.

- Reviewer of IEEE Embedded Systems Letters 2014.
- Reviewer of the journal "Mobile Networks and Applications" 2013.
- Reviewer for the following magazines: IEEE Micro 2012.

Session Chair

- Session "Dynamic Languages" at International Symposium on Code Generation and Optimization (CGO), 2020.
- Session "Performance Modeling and Prediction" at International Symposium on Performance Analysis of Systems and Software (ISPASS), 2019.
- Session "Parallelism and Concurrency" at International Symposium on Code Generation and Optimization (CGO), 2015.

Publicity Chair

- International Symposium on Code Generation and Optimization (CGO), 2017.

External Reviewer

- HPCA 2022, 2019, 2012
- ISCA 2024, 2020, 2019, 2017, 2016
- ASPLOS 2017, 2011
- MICRO 2014, 2012
- CGO 2014, 2013
- PACT 2010
- ICS 2011
- CCNC
- IEEE Consumer Communications and Networking Conference

Panel

- DOE Early Career CS/Systems Reviewer panel, 2022.
- NSF CCF Reviewer panel, 2022, 2020, 2018

Workshop/Forum

- Invited to attend to the Department of Energy Programming Systems Research Forum, 2022
- Invited to attend to the NSF Workshop on Future Directions for Parallel and Distributed Computing (SPX), 2019

Faculty Hiring Committee

- Computer Science Department, Northwestern University. 2023, 2022.
- Computer Engineering division of the Electrical and Computer Engineering Department, Northwestern University. 2023.

Ph.D. Admission Committee

- Computer Science Department, Northwestern University. 2023, 2022, 2021, 2020, 2019, 2018.
- Speaker for the visit day for incoming Ph.D. students. 2023, 2022, 2021, 2020, 2019, 2018.
- Organizer for the virtual visit day for incoming Ph.D. students in the Systems track of Computer Science. 2022.
- Speaker for the visit day for incoming Ph.D. students in the Systems track of Computer Science. 2023, 2022.

Ph.D. Thesis Committee

- Vijay Kandiah. Advisor: Nikos Hardavellas. Northwestern 2023.
- Enrico A. Deiana. Advisor: Simone Campanoni. Northwestern 2023.
- Brian Suchy. Advisor: Peter Dinda. Northwestern 2022.
- Spencer Florence. Advisor: Robby Findler. Northwestern 2020.
- Yuanbo Fan. Advisor: Russ Joseph. Northwestern 2018.
- Ali-Murat Gok. Advisor: Nikos Hardavellas. Northwestern 2018.
- Zhengyang Qu. Advisor: Yan Chen. Northwestern 2017.
- Georgios Tziantzioulis. Advisor: Nikos Hardavellas. Northwestern 2017.

Ph.D. Prospectus Committee

- Tommy McMichen. Advisor: Simone Campanoni. Northwestern 2024.
- Vijay Kandiah. Advisor: Nikos Hardavellas. Northwestern 2022.
- Brian Suchy. Advisor: Peter Dinda. Northwestern 2020.
- Enrico A. Deiana. Advisor: Simone Campanoni. Northwestern 2019.
- Xutong Chen. Advisor: Yan Chen. Northwestern 2019.
- Daniel Feltey. Advisor: Robby Findler. Northwestern 2018.
- Spencer Florence. Advisor: Robby Findler. Northwestern 2018.
- Xiang Pan. Advisor: Yan Chen. Northwestern 2017.
- Ali-Murat Gok. Advisor: Nikos Hardavellas. Northwestern 2016.
- Zhengyang Qu. Advisor: Yan Chen. Northwestern 2016.
- Georgios Tziantzioulis. Advisor: Nikos Hardavellas. Northwestern 2015.

Ph.D. Qualifying Exam

- Tommy McMichen. Advisor: Simone Campanoni. Northwestern 2023.
- Nick Wanninger. Advisor: Peter Dinda. Northwestern 2023.
- Enrico A. Deiana. Advisor: Simone Campanoni. Northwestern 2019.
- Ettore M. G. Trainiti. Advisor: Simone Campanoni. Northwestern 2019.

Master Thesis Committee

- Mercedes Sandu. Advisor: Ian Horswill. Northwestern 2024.
- Jasper Liang. Advisor: Simone Campanoni. Northwestern 2023.
- Drew Kersnar. Advisor: Simone Campanoni. Northwestern 2022.
- Michael Leonard. Advisor: Simone Campanoni. Northwestern 2019.
- Yian Su. Advisor: Simone Campanoni. Northwestern 2020.
- Qirui Luo. Advisor: Han Liu. Northwestern 2020.
- Jiayi Wang. Advisor: Han Liu. Northwestern 2020.

Other Committees

- Judge for the Student Research Competition (SRC) of the International Conference on Parallel Architectures and Compilation Techniques (PACT), 2022.
- Judge for the Student Research Competition (SRC) of the International Symposium on Code Generation and Optimization (CGO), 2020, 2017.
- Chair for the Student Research Competition (SRC) of the International Symposium on Code Generation and Optimization (CGO), 2018.
- Diversity Committee at Northwestern: 2024, 2023, 2022, 2021
- Graduate Program Enhancement committee: 2024, 2023, 2021, 2020

Talks

1. "Beyond Code-Centric Compilers: the Potential of Dependence-Centric and Memory-Centric Compilers".
   - Google. 2024.
   - Harvard. 2024.
   - Massachusetts Institute of Technology. 2024.
   - Argonne National Lab. 2024.
   - Politecnico di Milano. 2024.
2. "Evolving abstractions within and around compilers to support modern hardware and application trends".
   - ETH Zurich. 2023.
   - Politecnico di Milano. 2023.
   - Northwestern. 2023, 2022.
3. "NOELLE Offers Empowering LLVM Extensions".
   - the 19th International Symposium on Code Generation and Optimization (**CGO**), 2022.
   - Northwestern. 2022, 2021, 2020.
   - Princeton. 2020.
4. "X-CELLENT: X-Compiler Extending LLVM for Enhanced Natural Translation".
   - DOE. January 2022.
   - DOE project updates. June 2023, February 2023, September 2022, May 2022, February 2022.
5. "Evolving abstractions within and around compilers to better support current hardware and application trends".
   Presented at
   - Northwestern. March 2022, 2021, 2020, 2019, 2018.
   - ARM (virtual). December 2021.
6. "Introducing the Pseudorandom Value Generator Selection in the Compilation Toolchain".
   Presented at
   - the 17th International Symposium on Code Generation and Optimization (**CGO**), 2020.
7. "Liberating Threads from Non-Numerical Programs with an Architecture-Compiler Co-Design".
   Presented at
   - the ARM Summmit. Austin, Texas, USA. September 15-19, 2019.
8. "Time Squeezing for Tiny Devices".
   Presented at
   - the 46th International Symposium on Computer Architecture (ISCA). Phoenix, Arizona, USA. June 22-26, 2019. This talk was done together with Russ Joseph.
9. "My teaching approach".
   Presented at
   - Northwestern University at the annual award cerimony. June 7th, 2019.

10. "Deep Neural Networks Meet Compiler Technology".
    Presented at
    - Northwestern University at the Deep Neural Network Lab Kickoff Meeting. 2018.
11. "Compilers for the Post-Moore's Law Era".
    Presented at
    - Northwestern University, CS 496. 2020.
    - Northwestern University, CS 496. 2019.
    - Politecnico di Milano. 2018.
12. "Parallelization in the multicore era".
    Presented at
    - The Greater Chicago Area Systems Research Workshop (GCASR). 2016.
    - University of Massachussets, Northwestern, Harvard, Politecnico di Milano. 2015.
13. "The HELIX Parallelizing Compiler to Efficiently Manage Resources". Presented at the 13th International Conference on Hardware/Software Codesign and System Synthesis (**CODES+ISSS**), Amsterdam, Netherlands. October 6, 2015.
14. "HELIX-UP: Relaxing Program Semantics to Unleash Parallelization". Presented at the 12th International Symposium on Code Generation and Optimization (CGO). San Francisco, California, USA. February 7-11, 2015.
15. "Accelerating Sequential Code with the HELIX Parallelizing Compiler". Presented at Google. Cambridge, USA. November 11th, 2014. Invited talk.
16. "Should Compiler Designers (Re-)Focus on Extracting Parallelism?". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with ISPA). Milan, Italy. August 25th, 2014. Invited talk.
17. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs". Presented at the 41st International Symposium on Computer Architecture (ISCA), Minneapolis, Minnesota, USA, June 16, 2014.
18. "Breaking Cyclic-Multithreading Parallelization with XML Parsing". Presented at the 2nd International Workshop on Parallelism in Mobile Platforms (PRISM). Minneapolis, Minnesota, USA, June 14, 2014.
19. "The HELIX Project: Goal, Status, and Potentials". Presented at ARM. Cambridge, UK. January 29th, 2014. Invited talk.
20. "Extract Parallelism from Sequential Code for Current Commodity Multicore Processor". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with the 50th Design Automation Conference, DAC). Austin, Texas, USA. June 2nd, 2013. Invited talk.
21. "The HELIX Project: Overview and Directions". Presented at the 48th Design Automation Conference (DAC). San Francisco, California, USA. June 5th, 2012.
22. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing". Presented at the 10th International Symposium on Code Generation and Optimization (CGO). San Jose, California, USA. April 2nd, 2012.

23. “HELIX: The Importance of Predictability”. Presented at Princeton University - Princeton, USA. October 3, 2012. Invited talk.

24. “Static Memory Management within Bytecode Languages on Multicore Systems”. Presented at the Workshop on Computing in Heterogeneous, Autonomous ’N’ Goal-oriented Environments (CHANGE). Newport Beach, California. March 6th, 2011.

25. “ILDJIT: A compilation framework for CIL bytecode”. Presented at

    - Harvard University - Cambridge, USA. April 28, 2010.
    - Microsoft Research - Seattle, USA. March 22, 2010.

26. “Dynamic Compilation and Parallelism: Theory and large scale experimentation”. Presented at the PhD dissertation. Milan, Italy. March, 2009.

27. “Parallelism on compilation and execution”. PhDay at Politecnico di Milano. Milan, Italy. June 24th, 2009.

28. “Traces of control-flow graphs”. Presented at 13th International Conference on Developments in Language Theory (DLT). Stuttgart University, Germany. June 30, 2009.

29. “Dynamic Look Ahead Compilation: a technique to hide JIT compilation latencies in multicore environment”. Presented at 18th International Conference on Compiler Construction (CC). York, United Kingdom. March 24, 2009.

30. “A parallel dynamic compiler for CIL bytecode”. Presented at PhDay at Politecnico di Milano. Milan, Italy. June 26th, 2008.

31. “Traces of control-flow graphs: a feasibility study of using trace theory for compilation”. Presented at “Developments and New Tracks in Trace Theory” workshop, Cremona, Italy, October 11, 2008. Invited talk.

32. “Node-Level Optimization of Wireless Sensor Networks”. Presented at IEEE 2008 Wireless Communications, Networking and Mobile Computing (WiCOM). Dalian, China. October 13, 2008.

33. “Models and Tradeoffs in WSN System-Level Design”. Presented at IEEE 2008 International Conference on Digital System Design (DSD). Parma, Italy. September 4, 2008.

34. “Multi-level Design and Optimization of Wireless Sensor Networks”. Presented at IEEE 2008 International Conference on Networked Sensing Systems (INSS). Kanazawa, Japan. June 18, 2008.

35. “Ensuring Feasibility of Wireless Sensor Networks”. Presented at IEEE 2008 International Conference on Circuits and Systems for Communications (ICCSC). Shanghai, China. May 27, 2008.

36. “ILDJIT: a parallel dynamic compiler”. Presented at 16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC). Rhodes Island, Greece. October 14, 2008.

37. “SWORDFISH: a Framework to Formally Design WSNs Capturing Events”. Presented at IEEE 2007 International Conference on Software, Telecommunications and Computer Networks (SoftCOM). Split-Dubrovnik, Croatia. September 27, 2007.

38. “Common Language Infrastructure (CLI)”. Presented at Linux Day - Varese, Italy. October 5, 2007. Invited talk.

39. “Intermediate Language Distributed Just In Time for the CIL Bytecode”. Presented at the master thesis. Milan, Italy. July, 2006.

40. “DotGNU”. Presented at Linux Day - Sesto Calende, Italy. October 8, 2006. Invited talk.

41. “Ontology Packet Manager”. Presented at the bachelor thesis. July, 2004.

Teaching Experience

Course Instructor

I am passioned about teaching and I deeply care about making my students feel empowered by knowledge. My teaching philosophy and strategy that I apply in all my classes is briefly described here: link.
The table below is the evaluation obtained between all classes I thought at Northwestern University that have an evaluation from students.
Ratings in all tables below are between 1 (lowest) and 6 (highest). NA = Not Available.

Total number of students	*Rating of teacher*	*Rating of course*	*Amount learned*	*Intellectual challenge*	*Stimulating interest*
541	5.76	5.45	5.51	5.61	5.64

Northwestern University CS 322: Compiler Construction
Target: Undergraduate students
Hours taught: 50
Class website: link
Student comments: link
Student evaluation:

Year	*Number of students*	*Rating of teacher*	*Rating of course*	*Amount learned*	*Intellectual challenge*	*Stimulating interest*
2023 - 2024	41	5.77	5.42	5.43	5.57	5.67
2022 - 2023	42	5.84	5.44	5.50	5.50	5.74
2021 - 2022	30	5.92	5.79	5.79	5.64	5.93
2020 - 2021	21	5.88	5.78	5.89	5.78	5.88
2019 - 2020	28	5.83	5.61	5.78	5.72	5.83
2018 - 2019	32	5.45	5.18	5.23	5.55	5.33
2017 - 2018	18	5.91	5.55	5.82	5.82	5.91
2016 - 2017	20	5.82	5.64	5.55	5.55	5.82
2015 - 2016	14	5.67	5.60	5.80	5.20	NA
Average	27.33	5.79	5.56	5.64	5.59	5.64
Total	246					

Northwestern University CS 323: Code Analysis and Transformation
Target: Undergraduate and master students
Hours taught: 50
Class website: link
Student comments: link
Student evaluation:

Year	*Number of students*	*Rating of teacher*	*Rating of course*	*Amount learned*	*Intellectual challenge*	*Stimulating interest*
2023 - 2024	22	5.93	5.79	5.86	5.93	5.93
2022 - 2023	21	5.44	5.22	5.56	5.67	5.44
2021 - 2022	32	5.47	4.94	5.47	5.94	5.25
2020 - 2021	23	5.21	4.79	5.00	5.71	5.00
2019 - 2020	46	5.52	5.09	4.91	5.78	5.22
2018 - 2019	38	5.52	4.85	5.12	5.63	5.32
2017 - 2018	23	5.75	4.95	5.05	5.16	5.50
2016 - 2017	18	5.60	5.00	5.10	5.40	5.40
2015 - 2016	12	5.60	5.40	5.20	5.20	NA
Average	26.11	5.56	5.11	5.25	5.60	5.65
Total	235					

Northwestern University CS 397/497: Advanced Topics in Compilers
Target: Ph.D. and master students
Hours taught: 50
Class website: link
Student comments: link
Student evaluation:

Year	*Number of students*	*Rating of teacher*	*Rating of course*	*Amount learned*	*Intellectual challenge*	*Stimulating interest*
2023 - 2024	9	6.00	5.50	5.33	5.33	6.00
2022 - 2023	15	5.86	5.57	5.43	5.57	6.00
2021 - 2022	8	6.00	6.00	6.00	6.00	6.00
2020 - 2021	10	5.83	5.50	5.50	5.50	5.83
2019 - 2020	7	5.83	5.83	5.83	5.83	5.83
2018 - 2019	5	6.00	5.50	5.50	5.50	6.00
2017 - 2018	6	6.00	5.75	5.75	5.75	6.00
Average	8.57	5.93	5.66	5.62	5.64	5.64
Total	60					

Northwestern University The programming language and compilers week of CS 101 Computer Science: Concepts, Philosophy, and Connections.
Target: Undergraduate students.
Hours taught: 2.

- Fall 2019-2020: not available
- Fall 2018-2019: not available
- Fall 2017-2018: not available
- Fall 2016-2017: not available
- Fall 2015-2016: not available

Northwestern University CS 496 Introduction to Graduate Studies.
Target: First year PhD students.
Hours taught: 1.

- Fall 2021-2022: not available
- Fall 2020-2021: not available
- Fall 2019-2020: not available
- Fall 2018-2019: not available

Politecnico di Milano Computer Science Parallelism Course: Parallelism in wonderland: are you ready to see how deep the rabbit hole goes?
Target: Ph.D. students.
Hours taught: 20.
Student evaluation:

- Spring 2014-2015 with Prof. Marco D. Santambrogio: not available.

Harvard University Computer Science 253r: Virtual Machines.
Target: Ph.D. students.
Hours taught: 50.
Student evaluation:

- Fall 2010-2011 with Prof. Vijay Janapa Reddi: not available.

Teaching Assistance

November 2008 – January 2009 Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.
Target: Master students.
Hours taught: 10

November 2008 – January 2009 Formal languages and compilers course at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 10

March 2008 – July 2008 Software engineering at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 60

November 2007 – January 2008 Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.
Target: Master students.
Hours taught: 10

November 2007 – January 2008 Formal languages and compilers course at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 10

March 2007 – July 2007 Software engineering at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 60

November 2006 – January 2007 Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.
Target: Master students.
Hours taught: 10

October 2006 – January 2007 Informatica B laboratory at Politecnico di Milano university.
Target: Undergraduate students.
Hours taught: 20

Research Advising

ARCANA Rethinks Compiler Abstractions for New Applications research lab

Current Students

Ph.D. Students

2020 - Current Tommy McMichen

2021 - Current Yian Su

2022 - Current Federico Sossai

2022 - Current David Dlott

2023 - Current Haocheng Gao

2024 - Current Riley Boksenbaum

Undergraduate and Master Students

2024 - Current Benjamin Ye

Alumni

Ph.D. Students

2016 - 2023 Enrico Armenio Deiana
Ph.D. thesis: "Generating Thread-Level Parallelism in Nondeterministic Programs"
First position: Google

Undergraduate and Master Students

2020 - 2024 Brian Homerding

2024 - 2024 Jiarui Lu

2024 - 2024 Zachary Dale Gerstenfeld

2023 - 2024 Pengxiang Huang

2022 - 2024 Nathan Greiner

2022 - 2024 Riley Boksenbaum

2022 - 2023 Jasper Liang

2022 - 2023 Xiao Chen

2021 - 2023 Nikhil Kalghatgi

2022 - 2023 Tzu-Hsuan Huang

2021 - 2023 Kevin McAfee

2019 - 2021 Drew Kersnar

2021 - 2021 Alexandra Grimes

2021 - 2021 Siyuan Chai

2020 - 2021 Souradip Ghosh

2019 - 2020 Zhenqing Hu

2019 - 2020 David O'Sullivan

2019 - 2020 Lukas Gross

2018 - 2020 Yian Su

2016 - 2020 Ettore M. G. Trainiti

2018 - 2019 Jordan Timmerman

2018 - 2019 Michael Leonard

2018 - 2019 Angelo Matni

2018 - 2018 Sasha Weiss

2018 - 2018 Nathan John Shelly

2016 - 2016 Shrivant Bhartia

Advisor in Ph.D. Thesis

2023 *Enrico A. Deiana*. "Generating Thread-Level Parallelism in Nondeterministic Programs". Ph.D. in Computer Science, Northwestern University, Evanston, US. Committee = Simone Campanoni, Peter Dinda, Nikos Hardavellas, Robby Findler, Margo Seltzer, Arthur Maccabe (Barney).

Advisor in Master Thesis

2021 *Drew Kersnar*. "Number of Execution Analysis: Novel Relations to Facilitate Middle-End Instruction Scheduling". Master of Computer Science, Northwestern University, Evanston, US. Committee = Simone Campanoni, Peter Dinda.

2020 *Yian Su*. "A Better Memory Understanding for Program Dependence Graph through Static Value-Flow Analysis". Master of Computer Science, Northwestern University, Evanston, US. Committee = Simone Campanoni, Peter Dinda.

2019 *Michael Leonard*. "PRV Jeeves: A Study of Pseudorandom Value Generator Tradeoffs". Master of Computer Science, Northwestern University, Evanston, US. Committee = Simone Campanoni, Peter Dinda.

Co-advisor in Thesis

2012 *Pietro Malossi*. "Achieving Platform-Independence for the ILDJIT Compilation Framework". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2011 *Andrea Cazzaniga*. "Runtime threads managing in ILDJIT". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Marco Domenico Santambrogio.

2011 *Diego Mereghetti*. "Definizione di un supporto alla compilazione Just in Time nell'ambito dei sistemi auto adattativi". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Marco Domenico Santambrogio.

2010 *Luca Rocchini*. "Supporto alla programmazione generica nel compilatore ILDJIT". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Stefano Anelli*. "Method specialization for Common Intermediate Language in a dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Ettore Speziale*. "Multithreading support in ILDJIT dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Michele Tartara*. "ARM code generation and optimization in a dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Marcello Boiardi*. "Scelta automatica di algoritmi di ottimizzazione di codice all'interno del compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Cremona, Italy. Advisor: Prof. Pierluigi San Pietro.

2009 *Massimiliano Grandi*. "Supporto delle caratteristiche di introspezione dello standard ECMA-335 nel compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Cremona, Italy. Advisor: Prof. Pierluigi San Pietro.

2008 *Massimiliano Manni, Roberto Molteni*. "Progetto ed implementazione di librerie interne per il supporto dello standard ECMA-335 nel compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2008 *Alessandro Assinnata*. "Pianificazione di WSN". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. William Fornaciari.

Working Experience

September 2024	–	**August 2025**	Visiting Faculty Researcher at Google
September 2023	–	**Current**	Associate professor in the Computer Science Department of Northwestern University
September 2023	–	**Current**	Associate professor (by courtesy) in the Electrical and Computer Engineering Department of Northwestern University
August 2015	–	**August 2023**	Assistant professor in the Computer Science Department of Northwestern University
October 2019	–	**August 2023**	Assistant professor (by courtesy) in the Electrical and Computer Engineering Department of Northwestern University
June 2022	–	**November 2022**	Consultant for Ascenium
January 2020	–	**December 2020**	Co-director of the Center for Deep Learning of Northwestern University
November 2012	–	**July 2015**	Research Associate at Harvard University
November 2009	–	**October 2012**	Postdoctoral Position at Harvard University under both Prof. David Brooks and Prof. Gu-yeon Wei
August 2004	–	**September 2004**	Barman in Valencia, Spain
June 2002	–	**September 2002**	Kitchen assistant in Dublin, Ireland
July 2001	–	**April 2002**	Civil service at Gulliver in Cantello (Varese)
February 2001	–	**July 2001**	Industry worker at Suprema Oggiona S.Stefano building cash registers
July 2000	–	**January 2001**	Construction worker making hardwood floors
October 1999	–	**June 2000**	Pizza delivery driver
June 1999	–	**September 1999**	Industrial Electrician
June 1998	–	**September 1998**	Industrial Electrician
June 1997	–	**September 1997**	Industrial Electrician
June 1996	–	**September 1996**	Worked in a greenhouse

Software and Tools

2016 – Now Together with the rest of the **NOELLE** team, we developed the NOELLE compilation framework. This software is used in most research prototypes we have built since I have joined Northwestern University. NOELLE is also used in the https://users.cs.northwestern.edu/ simonec/ATC.html class

Website https://github.com/arcana-lab/noelle

Source Lines of Code: ∼ 45K of C++ 17, ∼ 2k of bash, 1k of Python.

2018 – Now Together with the rest of the team, we developed the GINO parallelizing compiler. This software is used in most research prototypes we have built that are about parallelism. GINO is also used in the https://users.cs.northwestern.edu/ simonec/ATC.html class

Website https://github.com/arcana-lab/gino

Source Lines of Code: ∼ 19K of C++ 17, ∼ 1k of bash, 1k of Python.

2015 – Now Developed the **VIRGIL** library, which is designed to be used by LLVM passes that generate parallel binaries. This library includes a customizable threadpool, a set of highly-optimized synchronization primitives and data structures. This library is currently used by the STATS compiler.

Website https://github.com/arcana-lab/virgil

Source Lines of Code: ∼ 4K of C++ 17

2017 – Now Developed **SIMO**. SIMO is a domain-specific language and its compiler to automatically generate websites and CVs. I use SIMO to automatically generate my website and my CV. The name means Sleeping In My Office (SIMO) because I developed it during nights spent in my office to avoid wasting time during the day where I prefer to focus on research challenges.

Source Lines of Code: ∼ 10K of C++ 17, ∼ 1K of bash script, ∼ 1K of AWK.

2015 – Now Developed ten LLVM passes that together implement an inter-procedural, alias analysis enhanced constant propagation for a domain-specific language. This software is used in the EECS 323 Code Analysis and Transformation class **CAT**

Website http://users.eecs.northwestern.edu/∼simonec/CAT.html

Source Lines of Code: ∼ 1K of C++ 14, ∼ 1k of bash.

2015 – Now Developed eight compilers from scratch that together create a compilation pipeline able to translate a subset of the C language down to Intel x86_64 binaries. This software is used in the EECS 322 Compiler Construction class **CC**

Website http://users.eecs.northwestern.edu/∼simonec/CC.html

Source Lines of Code: ∼ 40K of C++ 14, ∼ 1k of C, ∼ 3k of bash.

2015 – 2020 Together with Enrico A. Deiana, we developed the **STATS** compiler

Source Lines of Code: ∼ 13K of C++ 14, ∼ 2K of bash script, ∼ 2K of python 2.7

2017 – 2019 Developed a new backend for ARM in LLVM as well as three middle-end passes to build the **Time Squeezer** compiler

Source Lines of Code: ∼ 4K of C++ 14.

2010 – 2015 Developed a GPL licensed parallelizing compiler called **HELIX**

Website http://helix.eecs.harvard.edu

Source Lines of Code: ∼ 80K of C, ∼ 25k of C++, ∼ 15k of bash.

2005 – 2014 Developed a GPL licensed compilation framework called **ILDJIT** for the Common Language Infrastructure (CLI) described in the ECMA-335 standard.

Website http://ildjit.sourceforge.net

Source Lines of Code: ∼500k of C, ∼ 50k of C++, ∼ 10k of Python, ∼ 35k of bash, ∼ 7k of bison + flex, ∼ 3k of Ruby, ∼ 2k of Java.

2006 – 2008 Developed a GPL licensed framework to deploy automatically wireless sensors networks (**Swordfish**).

2005 – 2006 Extended the tuple-based middleware "TinyLime" to exploit sensors. The software has been used in the article "Pervasive games in a mote-enabled virtual world using tuple space middleware". Luca Mottola, Amy Murphy and Gian Pietro Picco. NetGames'06.

2005 – 2006 Developed a GPL licensed framework for developing agents based on the WSS project.

2004 – 2005 Developed a GPL licensed world simulator (WSS) for a GNU/Linux system to support the planning of sensor networks using a logic language as input.

2004 Developed a GPL licensed ontology packet manager for the GNU/Linux systems.

International Scientific Collaboration

Visiting experiences

January 2014 A week visit at University of Cambridge to collaborate with Dr. Timothy M. Jones and Prof. Robert Mullins in the context of the HELIX project.

August 2008 – November 2008 Three months visit at Harvard University. I have been involved in the ALARM research project, which is about the hardware process variation problem, under the supervision of Prof. Gu-Yeon Wei and Prof. David Brooks. I designed and implemented the code scheduler algorithm to dynamically reduce the fluctuation of the internal voltage of CPUs.

Participation in research projects

2007 – 2009 I have been involved in the OMP European research project at Politecnico di Milano. I was responsible to design and implement a dynamic compiler for the CIL bytecode language for ARM-based embedded platforms.

Institutions of past and current collaborators

- Northwestern University
- Princeton University
- Carnegie Mellon University
- University of Cambridge
- Harvard University
- Politecnico di Milano
- ARM
- ST Microelectronics
- INRIA

Education

January 2007 — March 2010 Ph.D. studies in Information Technologies at Politecnico di Milano.

Title: "A distributed Just-In-Time for CIL Bytecode".

My dissertation discusses theoretical and practical performance implications of thread level parallelism. To this end, I designed and built a bytecode virtual machine optimized for commodity multicore platforms. I am the author of ILDJIT, a parallel compilation framework that includes static and dynamic compilers as well as a bytecode virtual machine. ILDJIT has been used in several academic and industrial research projects, including the project HELIX that I started during my post-doc.

The Ph.D. was concluded with the highest honors. The advisor was Professor Stefano Crespi Reghizzi.

Sept. 2004 — July 2006 Engineering studies at Politecnico di Milano. I have been awarded the Master of Science (Laurea specialistica) degree in Computer Engineering (Ingegneria Informatica) with the highest honors (110 Lode). Details on the programs can be found at http://www.deib.polimi.it

During the studies, I developed a tuple based middle-ware extension for the TinyLime based on Lime and TinyOS that allows tuples to be sent on sensors.

In 2005-2006 I have worked on my thesis on an innovative project, building a new distributed virtual machine for the CLI architecture described in the ECMA 335 standard (DotNET). The thesis advisors were Prof. Stefano Crespi Reghizzi and Ing. Giovanni Agosta.

Sept. 2001 — July 2004 Engineering studies at Politecnico di Milano. I have been awarded the Bachelor of Science (Laurea triennale) degree in Computer Engineering (Ingegneria Informatica) with 108 out of 110 as final mark.

In 2004 I have worked on my thesis on an innovative project, building an ontology packet manager for the GNU/Linux systems. The thesis advisor was Prof. Marco Colombetti.

Sept. 1995 — July 2000 High-school education at ITIS of Gallarate "Roberto Franceschi" on Telecomunication and electronics.

School Participation

Summer 2007 ACACES: Summer School on Advanced Computer Architecture and Compilation for Embedded Systems

Miscellaneous

- ACM member
- IEEE member